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# A NOVEL COMBINATIONAL AND SEQUENTIAL CIRCUITS FOR LOW POWER APPLICATIONS

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***Abstract -*** Advanced computing systems infix Spintronic devices to boost the outflow performance of standard CMOS systems. High speed, low power, and infinite endurance area unit vital properties of magnetic tunnel junction (MTJ), a spintronics device that assures its use in reminiscences and logic circuits. This proposed design consists of a PentaMTJ-based gate that provides simple cascading, self-referencing, less voltage headroom downside in pre charge sense electronic equipment and low space overhead contrary to existing gates. PentaMTJ is employed here as a result of it provides warranted disturbance free reading and inflated tolerance to method variations at the side of compatibility with CMOS method. In this thesis both combinational and sequential circuits are designed with two different approaches. One is traditional CMOS based logic gates and anther one is PentaMTJ based logic gates. With the help of these two different types of logic design we have compared both traditional CMOS and PentaMTJ in terms of total no of transistors required for the design and how much power consumption required for the design. Design of XOR-XNOR gate is taken as an example of combinational circuit and Design of Gray Counter is taken as an example of sequential circuit. The gate is valid by simulation at the 120-nm technology in Microwind.

***Keywords -*** Counter, Spintronics, Magnetic logic gate, Magnetic tunnel junction.

## I. Introduction

The Spintronics is under research going on the process such as the nonvolatile and low power. The spin is used for storing data and the charge for its undertaking. It has the potential to interchange CMOS logic and memory. In extensive sub micrometer, scaling of CMOS source leakage power to dominate over all other power parts. Digital signals are interpreted in traditional CMOS logic by the absence and presence of electrical charge in terms of voltage or ground. But, in Spintronics, the digital signals are interpreted as up and down spin of electron. Spintronics devices are works on the principle of tunnel magneto resistance (TMR). Example of Spintronics device is Magnetic tunnel junction (MTJ).

An MTJ consists of two ferromagnetic layers and oxide layer which processes to improve the performance of CMOS logic circuits in terms of power dissipation; space needed, and interconnect delay. MTJ have two properties. Those are processing and storage. These two properties of MTJ used in order to reduce memory and interconnect delay or power but, MTJ have some drawbacks. In order to overcome MTJ drawbacks in the proposed design is implemented with PentaMTJ. PentaMTJ consists of two pinned ferromagnetic layer and one free layer. Pinned layer and free layer are separated by insulating oxide (MgO).

### A. Structure of PentaMTJ

A PentaMTJ is consisting of two pinned ferromagnetic layers and one free layer. In between the pinned layer and the free layer, MgO (insulating oxide) is used, as shown in Figure 1. Two resistance states, like in conventional MTJ, namely, one is a parallel state and the other is an anti parallel state. It is also effectively used in the realization of memory.

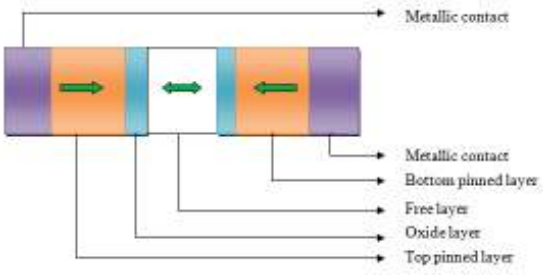


Fig. 1. Structure of PentaMTJ

PentaMTJ based realization of digital circuits has several benefits. First, PentaMTJ-based magnetic logic gates don't need referencing circuit because of pinned layers with opposite spin direction (self-referencing). Second, no additional hardware is required for complementary outputs because of the presence of pre charge sense electronic equipment (PCSA) for sensing. Third, the output of a Spintronics device is directly detected by the PCSA therefore there does no have to be compelled to initialize the state of the output MTJ for sensing.

The sensing power consumption is reduced and the speed is enhanced due to the use of PCSA as sense amplifier because it turns ON only for a short duration during the transitions. Finally, ease of cascading is the greatest contribution of our proposed magnetic logic gate

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because the output of the gate and the programming signal of PentaMTJ are both voltage signals.

## II. Literature Survey

### A. Recent developments in magnetic tunnel junction MRAM

In this paper reviewed our evolution on Magneto resistive Random Access Memory (MRAM) based on Magnetic Tunnel Junctions (MTJ). We have indicated MTJ element in the 1–1000 kΩ-um2 range with MR values above 40%. The switching characteristics are mainly driven by the magnetic shape anisotropy that appears from the element boundaries. The switching repeatability, along with hard axis selectability, is shown to be dependent on both shape and aspect ratio. MTJ memory parts were successfully integrated with 0.6 um CMOS technology, achieving read and program address access times of 14 ns in a 256 2 MRAM. Magneto resistive Random Access Memory (MRAM) based on integration of Magnetic Tunnel Junction (MTJ) and CMOS has the potential to be competitive with existing semiconductor memories. Key aspects of MRAM technology are non volatility and unlimited read and write endurance. In addition, it is anticipated that MRAM could operate at high speed and low voltage, with comparable densities. Controlling the resistance regularity, switching behavior of magnetic bits, and integration of MTJ with CMOS are some of the key challenges to successful implementation of this technology.

### B. Magnetically engineered spintronic sensors and memory

The discovery of enhanced magneto resistance and oscillatory interlayer exchange coupling in transition metal multi layers just over a decade ago has enabled the development of new classes of magnetically engineered magnetic thin-film materials suitable for advanced magnetic sensors and magnetic random access memories. Magnetic sensors based on spin-valve giant magneto resistive (GMR) sandwiches with artificial anti ferromagnetic reference layers have resulted in enormous increases in the storage capacity of magnetic hard disk drives. The unique properties of magnetic tunnel junction (MTJ) devices has led to the development of an advanced high performance non volatile magnet random access memory with density approaching that of dynamic random access memory(RAM) and read write speeds comparable to static RAM. Both GMR and MTJ elements are examples of spintronic devices in which the flow of spin-polarized electrons is employed by controlling, via magnetic fields, the direction of magnetic moments in homogeneous magnetic thin film systems. More complex devices, considering three-terminal hot electron magnetic tunnel transistors, suggest that there are many other applications of spintronic materials.

### C. Magnetic adder based on racetrack memory

The downplay of integrated circuits based on complementary metal oxide semiconductor (CMOS) technology meets a significant slowdown in this decade due to several technological and scientific difficulties. Spintronic devices such as magnetic tunnel junction (MTJ) nanopillar become one of the most promising candidates for the next generation of memory and logic chips thanks to A magnetic processor based on spintronic devices is then expected to overcome the issue of increasing standby power due to leakage currents and high dynamic power dedicated to data moving. The proposed multi-bit MA circuit promises nearly zero standby power, instant ON/OFF capability, and smaller die area. By using an accurate racetrack memory spice model, we validated this design and simulated its performance such as speed, power and area, etc.

## III. Proposed Work

The proposed structure of PentaMTJ needs less current for writing as compared with the conventional MTJ. It requires current only for converting antiparallel to parallel state for one stack, the other stack automatically comes into antiparallel state. The effect of process variation of one stack is nullified by another stack in case of PentaMTJ contrary to two different MTJs whose process variations degrade the performance. Actually, no experimental data is available for the double barrier and therefore, we have assumed that the single barrier model is also valid for a double barrier for TMR ratio.

PentaMTJ has lower resistance than the conventional MTJ because it works well for small value of oxide thickness compared with MTJ. The spin-transfer torque using perpendicular magnetic anisotropy (PMA) would greatly reduce the required switching voltage due to the absence of the easy-plane anisotropy term found in in-plane devices which increases the switching voltage without contributing to the activation energy.

### A. Logic in memory

The logic-in-memory architecture, shown in Figure 2, is composed of three parts:

1) PCSA for sensing the difference between the two states of resistance.

2) PentaMTJ logic, and

3) PentaMTJ writing cell

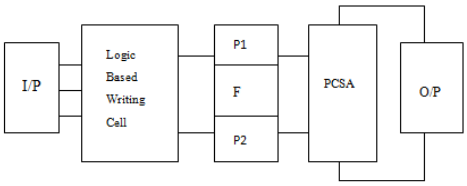



Fig.2. Block diagram of logic gate based PentaMTJ

PCSA is a dynamic logic circuit having two phases, namely, a precharge phase and an evaluation phase. The discharging of both branches of PCSA depends upon their relative resistances such that the low-resistance branch discharges the output node capacitance more rapidly that cuts off the other branchbecause of the cross-coupled PCSA structure.

### B. Design Of 4-Bit Gray Counter

Sequential logic circuits differ from combinational logic circuits as the output of a sequential logic circuit depends upon both the previous output (present state) and the present input. A 4-bit Gray counter is a sequential circuit whose successive states differ in only one digit. The present state in a sequential circuit like Gray counter is stored in flip-flops, which is very power consuming under standby condition. Use of MTJ/PentaMTJ in a sequential circuit is beneficial because in case of unintentional shutdown, the counter can be restored from its previous state instead of its initial state. The previous state is rebuilt from PentaMTJ within few hundred picoseconds. In the Gray counter, PCSA is used for sensing to generate the next state, PentaMTJ for present state storage and the writing circuitry to assign the next state to the present state.

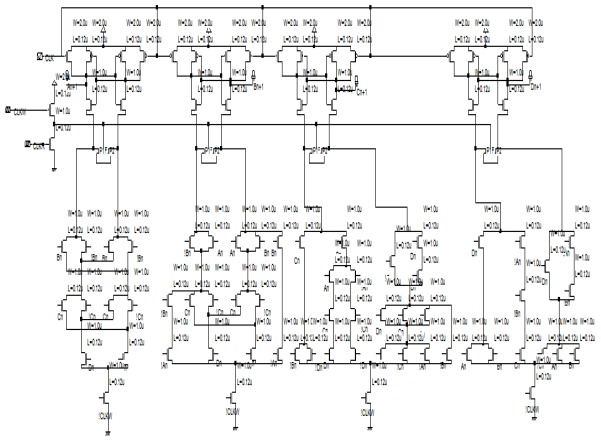


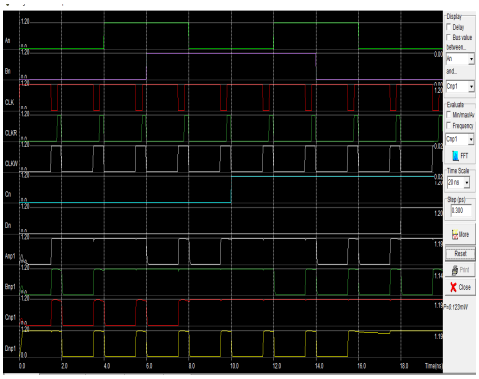
Fig.3. Circuit diagram of 4-bit gray counter using PentaMTJ

Fig 3 shows the circuit diagram of a 4-bit Gray counter comprising of four PentaMTJs for storage, three PCSAs for sensing, and a writing circuit according to the characteristic Eq. 1. $A_{n+1}$, $B_{n+1}$, $C_{n+1}$ and $D_{n+1}$ are evaluated using K-map. $A_n$, $B_n$, $C_n$ and $D_n$ are the inputs and $A_{n+1}$, $B_{n+1}$, $C_{n+1}$ and $D_{n+1}$ are outputs.

$$A_{n+1} = [C_n \oplus D_n] \odot B_n$$
$$B_{n+1} = [C_n \odot D_n]\,[A_n + B_n] + \bar{A}_n B_n$$
$$C_{n+1} = C_n[\bar{D}_n + \bar{B}_n] + B_n[A_n C_n D_n + \bar{A}_n \bar{C}_n \bar{D}_n]$$
$$D_{n+1} = D_n[A_n + B_n] + C_n \bar{A}_n \bar{B}_n$$

It starts operating by writing in PentaMTJ using the clock CLKW with a pulse width of 1.5 ns. To accomplish the writing in PentaMTJ in 1.5 ns, a clock CLKW with 2-ns time period and 1.5-ns pulse width is generated. The pre charging and then sensing are performed when CLKW is high (500 ps) using a short duration low CLK (300 ps) pulse followed by a short duration high CLKR pulse (200 ps). The same process is repeated until the counter stops. Fig 4 shows the simulation results with $A_{n+1}$ being the least significant bit and $D_{n+1}$, the most significant bit.

## IV. Simulation Result



Voltage vs time

Fig.4. Simulation result of 4-bit gray counter using PentaMTJ

## V. Conclusion and Futurescope

The no of transistors required for the design of combinational circuit using PentaMTJ is more compared to traditional CMOS logic design. But, the power consumption of PentaMTJ is less compared to traditional CMOS design. Hence, low static power, short interconnect delay are the attractive features of PentaMTJ. PentaMTJ logic decreases the area overhead by reducing the number of transistors required for design of traditional CMOS based logic gates. And also the total number of bits increased in the design of sequential circuit using PentaMTJ has less number of transistors and low power consumption compared to CMOS based sequential circuit. PentaMTJ also provides guaranteed disturbance free reading and increased tolerance to process variations due to its differential nature.

In this paper 4-bit PentaMTJ based gray counter is designed and implemented .We have got reduced power dissipation compared to CMOS based gray counter. In future PentaMTJ based gray counter designed and implemented with increased no of bits so we can achieve less power compared to CMOS based gray counter.

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