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POWER AND ENERGY EFFICIENT FLIP-FLOPS USING FLOATING GATE AND QUASI FLOATING GATE TECHNIQUES AT 180NM

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ABSTRACT

The objective of this research is to know the effectiveness of floating gate technique and quasi floating gate technique on various types of flip flops on lowering power dissipation, propagation delay and/or power delay product.The analysis is done on the experimental results obtained using Cadence virtuoso simulator at 180nm CMOS technology. It is found that the propagation delay is reduced by 76% and PDP is reduced by 77% in Dual edge Triggered Flip Flop with floating gate technique. The PDP is reduced by 45% with quasi floating gate technique in this flip flop. The reduction in PDP is 47% with floating gate technique in TSPC flip flop. With quasi floating gate technique, this reduction in PDP is 68.7% in TSPC flip flop. In semi dynamic flip flop the reduction in PDP is only 0.8% with floating gate technique and almost negative impact of quasi floating gate technique. For the first time this study finds an impact of FG and QFG techniques in various types flip flops in reducing power dissipation and PDP at 180nm technology node. This study could further be extended in subthreshold region for further reduction in power dissipation and PDP. Also this study shows that FG and QFG is not always effective in reducing power and effectiveness varies from circuit to circuit. This reason could be analyzed further as the future scope of the paper.

KEYWORDS : Dual edge triggered Flip Flop, Semi dynamic Flip Flop, True single phase clocking, Floating gate technique

There are so many techniques used to reduce or minimize delay and power dissipation in electronics designs. Floating gate and quasi-floating gate techniques have own importance in designs. It depends on circuit to circuit, how to minimize delay or power dissipation of circuits. Now, we are going to study advantages of these techniques. We have three types of flip-flops i.e. dual edge triggered, true single phase clocking and semi-dynamic.

Floating gate technique is used in both analog and digital circuits. The FGMOS differs by a conventional MOSFET in that it has multiple input gate terminals, which is fully isolated with oxide. It required less delay to simulate as compare to conventional circuit. Circuit can operate at supply voltage level which is below the intended operational limits (Joshi et al., 2013). It consumes less power. Some advantages of FGMOS are: compatible with standard CMOS technology, ability to shift signal levels, ability to reduce complexity of designs, programmable threshold voltage. FGMOS is to rise the operating range of low input and out compliance voltages, resultant a low equipment weight (Badwal et al, 2014).

The quasi floating gate circuit is defined by the special combination of the circuit with floating gate transistor. The FGMOS designs required large area and high leakage on the floating gate that's why we use quasi floating gate. It offers better performance of frequency response, offsets and chip area. It has high frequency with low noise effect (Bonakpour and Razaghian, 2013).

VARIOUS FLIP-FLOPS TYPES USED

Dual Edged Triggered Flip-Flop

The sample data on the positive and negative edges of the clock is operated onone half of the clock frequency to save energy. Drawbacks are: it increases the skew of negative edges in sensitivity of duty cycle variation.DET has half the clock frequency and two times activity factor. Energy dissipation in flip flop is remains same. In circuit system, energy is prevailed by register and not by clock share. It lends to have some problems in area, delay and energy.

Figure 1 shows two separate master latches operates on opposite phase of clock. The multiplexerused instead of slave latches. Figure 2 shows a CMOS implementation of design. In pulse generator a pulse lies on both edges of clock. The transistorsbased design used in a pulsed latch. It is an efficient pulse generator (Neil and David, 2011).

True Single Phase Clocking Flip-Flop

Several techniques used for minimize repetition of clock system. TSPC flip-flops requiredless areadue to small number of transistor. By some changes in internal switching of these flip-flops, so that it will minimize power dissipation. The circuit comprised of changing levels of n-blocks and p-blocks driven by the one clock pulse. The CMOS implementation of standard TSPC flip-flop is shown in Figure 3 (Sharma and Mehra, 2014). When the clock

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signal is 0, then input is come from the output. When clock is 0 to 1, then output will be latch the reverse of the input. The CMOS implementation of TSPC flip-flop with 11 transistors used byone clock signal.

Semi-dynamic Flip-Flop

A connection between a flip-flopand a pulsed latch. As pulse latch, it based on priciple of interfering pulses.It uses a dynamic NAND gate instead of static NAND. When clock is 0, X precharge high, Q holds the old state,When clock gets incseaed, Dynamic NAND computes.If D is 0, X is unchanged and nmos transistor gets OFF. If D is 1, X gets low, the trasistor still ON to complete transist response. This will make tohold time for a short pulse. The first block is shown as master latch and the second block is shown as the slave. The SDFF allows rising input and falling input at after the rising clock edge and at before the rising clock edge respectively. It operates the dynamic inputs stage along with static operation, so it is known as semi dynamic. SDFF is somewhat faster as compare to pulse latch. But it left withonly skew tolerance and time borrowing capacity. It has also high energy consumes because large number of nodes with high activity factor. Figure4 shows the circuit of semi-dynamic flip-flop (Neil and David, 2011).

MATERIALS AND METHODS

In this experimental study various types of CMOS Flip Flops are simulated with Cadence Virtuoso simulator with 180nm technology CMOS model. These flip flops are simulated with floating gate technique and quasi floating gate technique to know the impact on power dissipation, PDP etc. and the results are compared with conventional simple circuit without any technique.

RESULTS

Table 1 shows the value of propagation delay, power dissipation and PDP of simple dual edge triggered flip-flop and row 2 and row3 are the results of this FF with FG and QFG technique. Figure 5 shows the waveform of the 3 types of FF without any technique. Figure 6 shows the waveform of the 3 types of FF with FG technique. Figure 7 shows the waveforms of these 3 types FF with QFG technique. Table 2 shows the PD, power and PDP for TSPC flip-flop without any technique and with FG and QFG technique. Similarly Table 3 is showing the same parameters for semi-dynamic FF with FG, QFG and without any technique.

DISCUSSION

In FG technique, the values of R and C are 1 M ohm and 1 uF respectively. In QFG technique, the value of C is 1 pF. As can be seen in rows 2 and 3 of table 1 and table 2 of the these FFs, there is reduction in power dissipation for sure in FG technique and also reduction in PDP. But sometimes FG and/or QFG techniques are not effective in reducing power, propagation delay or PDP as can be seen in row2 and row3 of table 3 of semi dynamic FF. In these cases, QFG technique is used to reduce the area of a circuit as diodes are used in place of resistors. It is well known fact that resistors require large area. Waveforms shown in the figure 5, 6 and 7 of these FFs with FG and QFG techniques confirm the results tabulated in 3 tables.

CONCLUSION

In this paper, FG and QFG based various types of flip-flops have been proposed and analysed to show its advantages and suitability for low power application. Propagation delays and power dissipation of these techniques varies from circuit to circuit. As we can see that FG and QFG of DET and TSPC flip-flops are better than conventional circuit in both parameters, but in semi-dynamic flip-flop, delay and power dissipation of FG is almost equal to conventional and propagation delay of QFG is greater than conventional .So sometimes FG and QFG techniques are ineffective to reduce propagation delay and power.

Initially we had worked on FG technique but it has drawback that it requires more area because of large value of resistors. Keeping this in mind, we tried QFG technique instead of FG technique to make area efficient but it consumes much power because of active components i.e. diodes. Most of the times, FG technique results in low propagation delay as well as low power dissipation, so it is well suited for many analog/digital signal processing circuits. These circuits could also be studied further in subthreshold region with forward and reverse body biasing techniques for further reduction in power and propagation delay. This is the future scope of this research work

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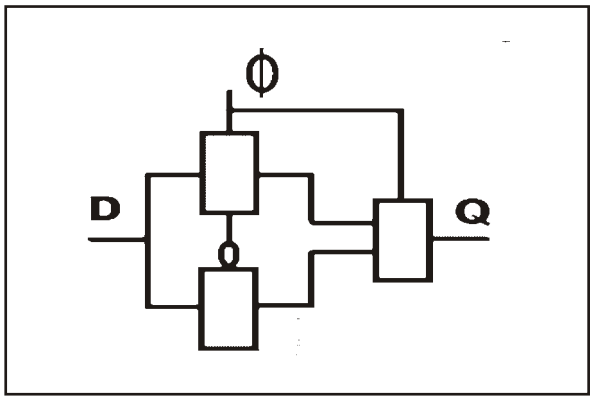

Figure 1: Block diagram of Dual Edge triggered FF

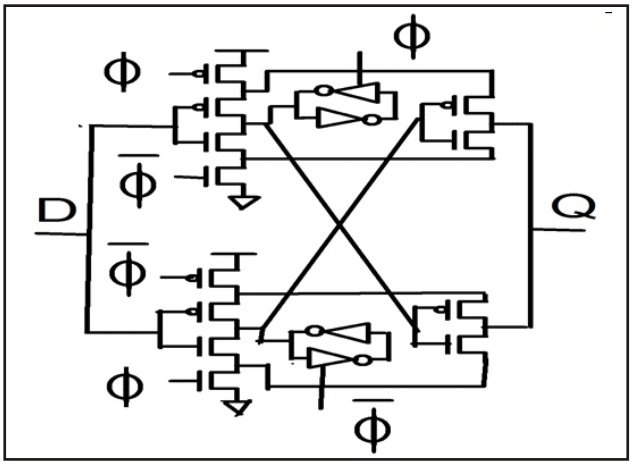

Figure 2 : Trasisitor level implementation of DET Flip-Flop

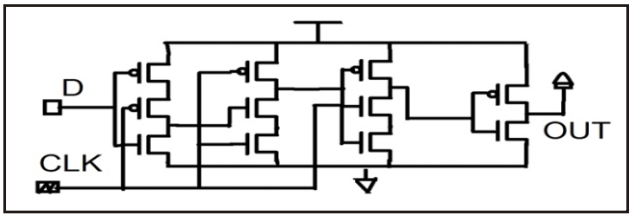

Figure 3: True single phase clocking Flip-Flop

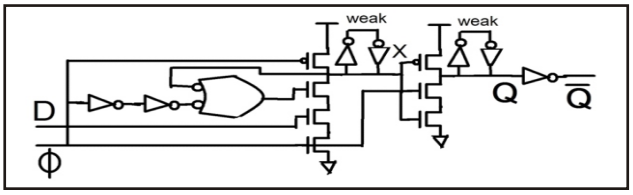

Figure 4: Semi dynamic Flip-Flop

Table 1: Dual edge triggered Flip-Flop parameter comparisons

Types	P. Delay (Secs)	Power Diss (Watts)	ENERGY (Joules)
Conventional	289.2×10^{-12}	8.7383×10^{-4}	2.54×10^{-13}
FG	69.58×10^{-12}	8.528×10^{-4}	5.93×10^{-13}
QFG	227.3×10^{-12}	6.152×10^{-4}	1.39×10^{-13}

Table 2: TSPC Flip-Flop parameter comparisons

Types	P. Delay (Secs)	Power Diss (Watts)	ENERGY (Joules)
Conventional	58.22×10^{-12}	9.925×10^{-5}	5.77×10^{-15}
FG	55.98×10^{-12}	5.471×10^{-5}	3.06×10^{-15}
QFG	56.084×10^{-12}	3.225×10^{-5}	1.81×10^{-15}

Table 3: SD Flip-Flop parameter comparisons

Types	P. Delay (Secs)	Power Diss (Watts)	ENERGY (Joules)
Conventional	18.48×10^{-12}	1.324×10^{-3}	2.44×10^{-14}
FG	18.29×10^{-12}	1.324×10^{-3}	2.42×10^{-14}
QFG	25.01×10^{-12}	1.281×10^{-3}	3.21×10^{-14}

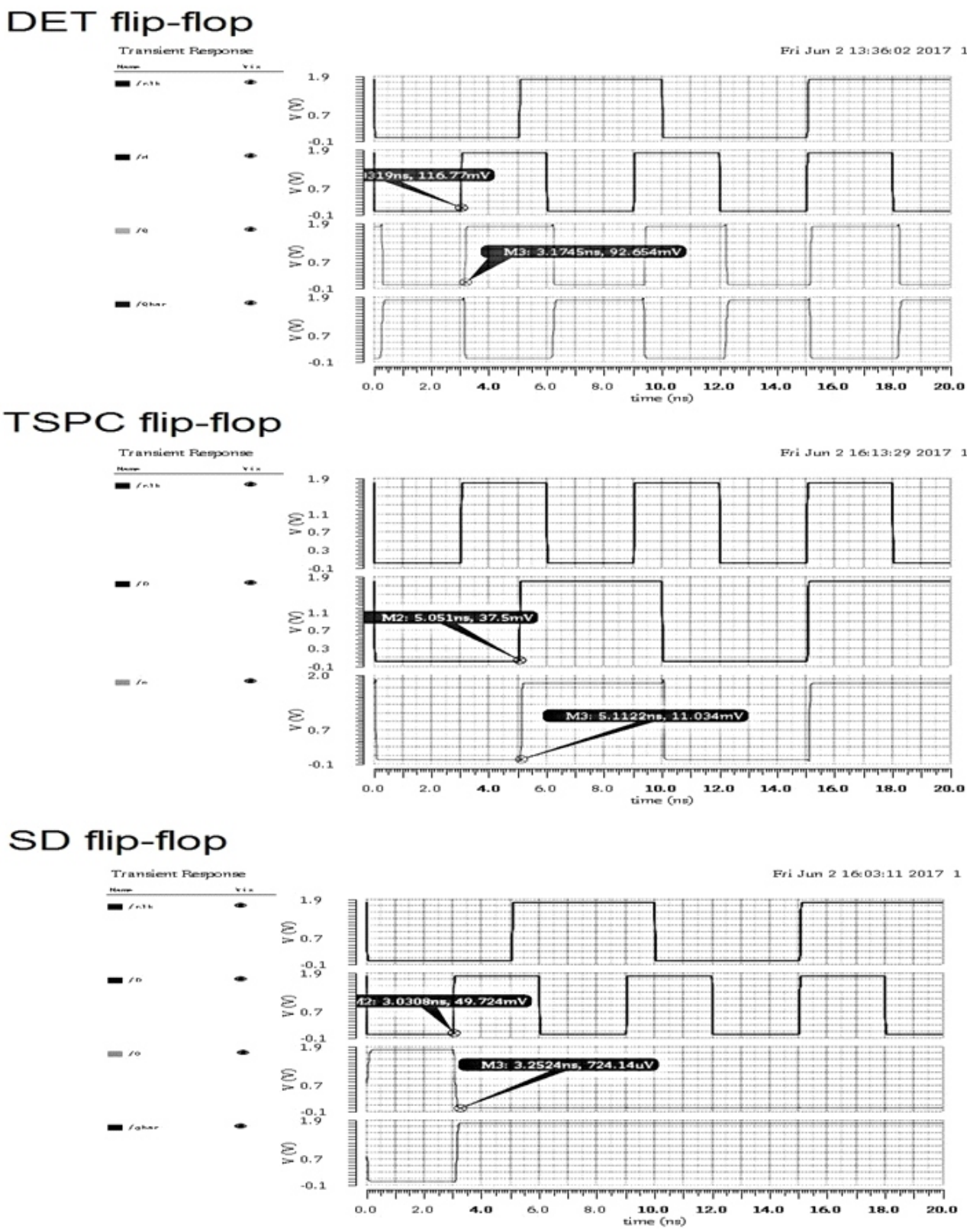

Figure 5: Waveforms of Conventional flip-flop

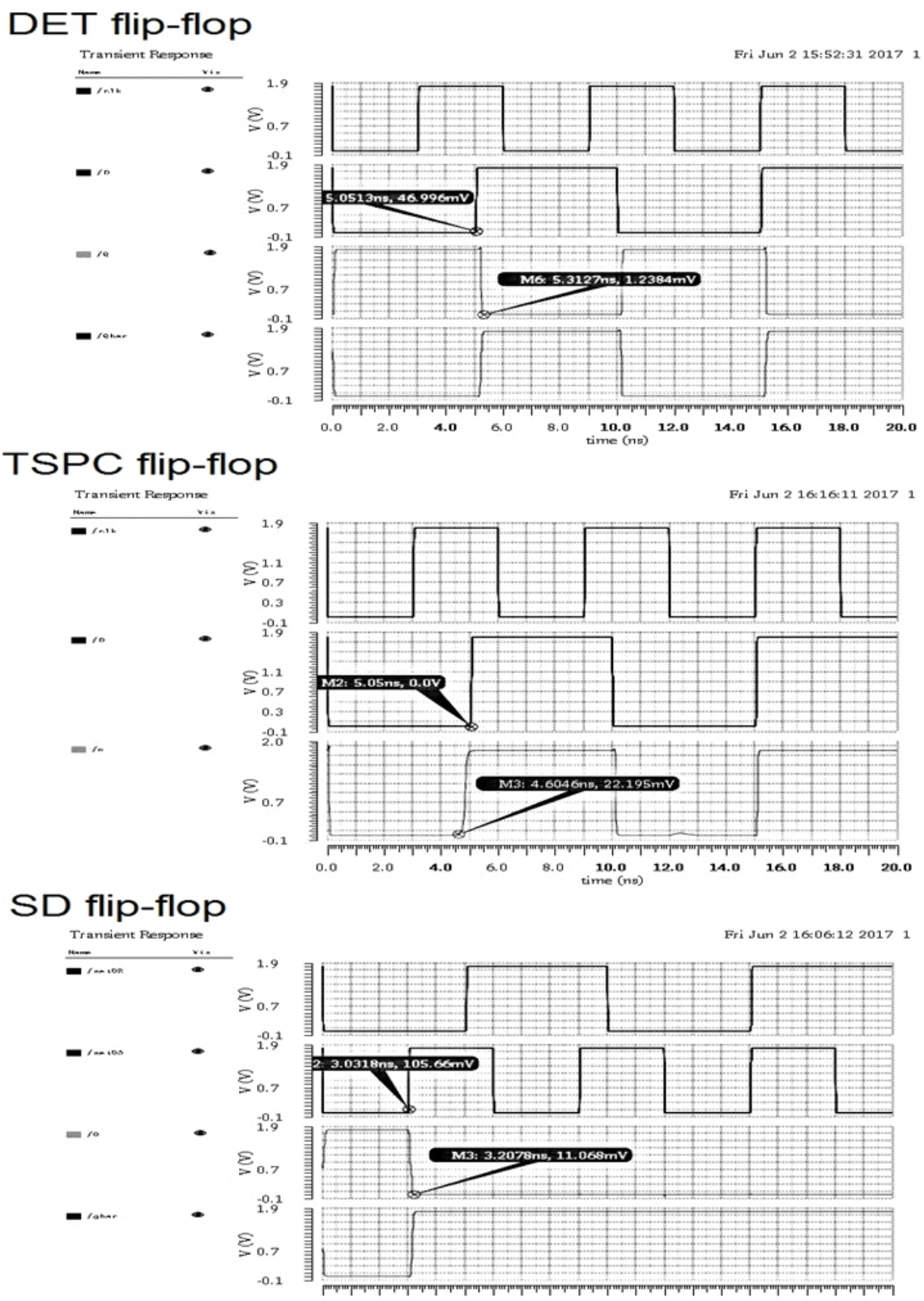

Figure 6: Waveforms of FG based flip-flop

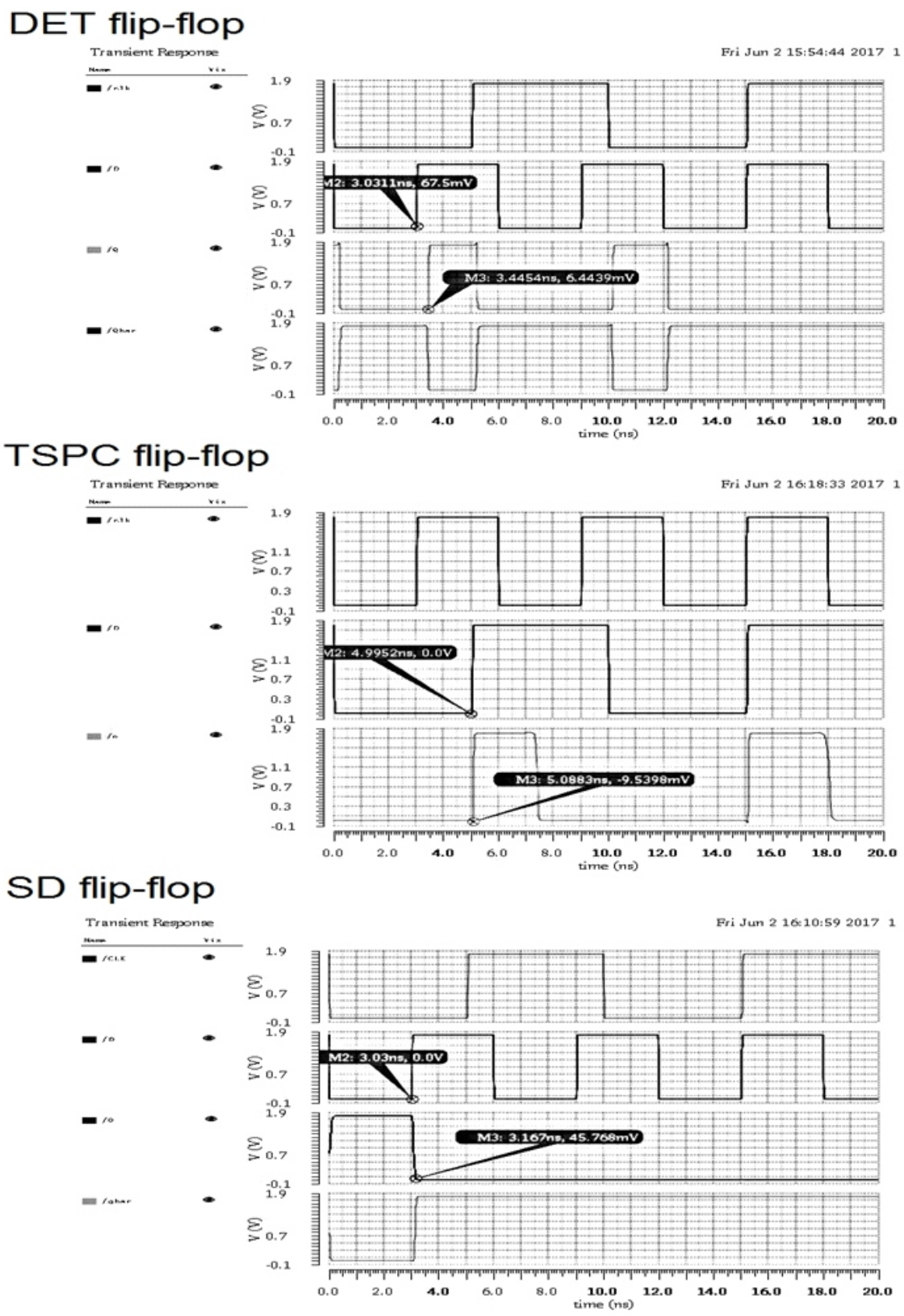

Figure 7: Waveforms of QFG based flip-flop

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