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MAC BASED AN ADAPTIVE EDGE DETECTION FILTER FOR IMAGE PROCESSING APPLICATIONS ON FPGA

[1]A. Bhavana, [2]Mohd Imaduddin
[1]VLSI System Design, Aurora's Scientific, Technological and Research Academy, Bandlaguda, Hyderabad. Telangana
[2]Head of the Department, Department of Electronics and Communication Engineering, Aurora's Scientific, Technological and Research Academy, Bandlaguda, Hyderabad. Telangana

Abstract-An adaptive edge detection filter has been introduced for image processing applications. And important point is the proposed filter works uniquely compare to other existing filter due to its properties. A new approach is proposed for edge detection in image processing applications .By using fully parallel and fully pipeline MAC (Multiply and Accumulate) concept which can implemented on FPGA tool kit. This provides area, cost, and performance efficiencies with respect to other methods. Filter is designed using Xilinx DSP tools, MATLAB and synthesized with ISE 10.1 and implemented on vertex II pro based 2V0ffll48-7 FPGA device. Partial results like blurring of images are shown.

Keywords- Edge detection, MAC, Mat lab, ISE

I. Introduction

Digital images play an important role, both in daily life applications such as satellite television, magnetic resonance imaging, computer tomography as well as in areas of research and geographical information system and anatomy. An image is a 2D representation of a three dimensional scene .A digital image is basically a numerical representation of an object. The term digital image processing refers to the manipulation of an image by means of a processor. A very important goal of the computer image analysis and processing is to generate some particular images that are more suitable for people or machines to observe and identify.

Image edges are the most basic features of an image. The so called image edge refers to the most prominent part of partial intensity changes in images. Digital image processing is a subset of the electronic domain, wherein the image is converted to an array of small integers, called pixels, representing a physical quantity. Edges characterize boundaries and edge detection is one of the most difficult tasks in image processing hence it is a problem of fundamental importance in image processing. The problem of edge detection although it is fundamental and is existing since years but it is still an area where there is still scope of research. It has been found that the previous used algorithms or methods were not able to produce ideal or optimized results. An edge detection method applicable to gray level images in which an objective function is used to extract edge points as well as their directions.

Edge detection is in the forefront of image processing. For object detection, it is crucial to have a good understanding of edge detection algorithms. It is one of the most commonly used operations in image analysis. An edge is the boundary between an object and the background. In this section, work done in the area of edge detection is reviewed and focus has been made on detecting the problems of the previous work done. The most commonly used methods for edge detection include Sobel, Prewitt, Kirsch and canny operators. Edge detection is a basic and important subject in computer vision and image processing techniques applied in edge feature extraction. It is a kind of issues which are unable to resolve completely so far.

A new approach is proposed in this paper for edge detection in image processing applications .By using fully parallel and fully pipeline MAC (Multiply and Accumulate) concept which can implemented on FPGA tool kit. This provides area, cost, and performance efficiencies with respect to other methods.

In Section II edge detection concept is discussed, section III and IV shows the proposed method and system design. Implementation of proposed system and obtained results are discussed in section V. Finally Conclusions and future work are discussed in section VI.

II. Related Work

The Edge is a set of those pixels whose grey have step change and rooftop and exist between the main objectives and goals, Objectives and background and regional and regional. Edge detection is a basic and important subject in computer vision and image processing techniques applied in edge feature extraction. It is a kind of method of image segmentation based on range non continuity. Image edge detection is one of the basal contents in the image processing and analysis and also is a kind of issues which are unable to resolve completely so far. Goal of Edge Detection is detection and Localization of Image Edges. An edge is a property attached to an individual pixel and is calculated from the image function

[1]Corresponding Author

behavior in a neighborhood of the pixel. Edge information in an image is found by looking at the relationship a pixel has with its neighborhoods. If a pixel's gray-level value is similar to those around it, there is probably not an edge at that point. If a pixel's has neighbors with widely varying gray levels, it may present an edge point.

Various edge detection filters are discussed bellow,

A. Median filter

The median filter is a non-linear filter that has been used successfully in a variety of domains. Its strength lies in its ability to filter out impulsive noise without destroying the properties [1] of the underlying signal. In the image processing domain, this is manifested in edges remaining intact The Trace Transform is used to give an alternative representation of the image, useful for recognition and authentication systems. In each case, the number of sample points can be over 100,[1] depending on the size of the image in question. Furthermore, the number of samples of interest can vary as the lines cross the image at varying angles.[3] Hence a scalable method of median calculation is needed, which must also cope with variable window size.

B. An Area Efficient Alternative to Adaptive Median Filter

A new approach to the FPGA implementation of image filters are made ,which are utilized to remove the salt pepper noise of high intensity i.e. up to 70% corrupted pixels using evolutionary algorithm with simple human designed pre-processing [2]and post-processing unit. The goal is to provide designs and conventional designs are able to significantly reduce the overall implementation cost on a chip in comparison to standard approaches based on sophisticated filtering schemes such as adaptive medians.

C. Sobel Operator And Genetic Algorithms

Edge detection of images is a classical problem in computer vision and image processing. The key of edge detection is the choice of threshold; the choice of threshold directly determines the results of edge detection. How to automatically determine an optimal threshold [3]is one of difficult points of edge detection. In this paper, Sobel edge detection operator and its improved algorithm are first discussed in term of optimal threshold. Then based on genetic algorithms and improved Sobel operator, a new automatic threshold [3] algorithm for images processing is proposed. Finally, the edge detection experiments of two real images are conducted by means of two algorithms.

D. Canny Edge Detection Algorithm

The Canny edge detection algorithm is known to many as the optimal edge detector. The first and most obvious is low error rate. It is the important that edges occurring in images should not be missed and that there are no responses to non-edges. The second criterion is that the edge points be well localized. A third criterion is to have only one response to a single edge. This [4] was implemented because the first two were not substantial enough to completely eliminate the possibility of multiple responses to an edge. was based on a step edge corrupted by additive white Gaussian noise. Canny edge detection developed an approach to derive an optimal edge detector based on three criteria related to the detection performance.

E. FPGA Implementation of High Speed FIR filters Using Add and Shift Method

A method for implementing high speed Finite Impulse Response (FIR) filters using just registered address and hardwired shifts. FPGAs are being increasingly used for a variety of computationally intensive applications, mainly in the realm of Digital Signal Processing (DSP) and communications. Due to rapid increases in the technology, current generation of FPGAs contain a very high number of Configurable Logic Blocks (CLBs), and are becoming more feasible for implementing a wide range of applications.

III. Proposed Method

FPGA based efficient design of an adaptive edge-detection filter for image processing application has been presented. The FPGA implementation provides the necessary performance for real-time image and video processing, while retaining the system flexibility to support an adaptive algorithm. A fully parallel fully pipelined MAC algorithm is used to implement the proposed filter. This approach is useful to enhance the system performance by taking optimal advantage of embedded Multipliers, BRAMs and Registers available on target FPGA.

An adaptive edge-detection algorithm is necessary to provide a robust solution that is adaptable to the varying noise levels of these images to help distinguish valid image content from visual artifacts introduced by noise.

An embedded FPGAs offer a very attractive solution that balance high flexibility, time-to-market, cost and performance. Therefore, an area and power efficient adaptive edge detection filter is implemented on target FPGA using multiply and accumulate (MAC) technique. There is a constant requirement for efficient use of FPGA resources where occupying less hardware for a given system can yield significant cost-related benefits like:

(i) Reduced power consumption

(ii) Area for additional application functionality

(iii) Potential to use a smaller, cheaper FPGA

This process detects outlines of an object and boundaries between objects and the background in the image. An edge-detection filter can also be used to improve the appearance of blurred or anti-aliased video streams. The basic edge-detection operator is a matrix area gradient operation that determines the level of variance between different pixels. The edge-detection operator is calculated by forming a matrix centered on a pixel chosen as the center of the matrix area. If the value of this matrix area is above a given threshold, then the middle pixel is classified as an edge.

A fully parallel fully pipelined MAC algorithm is used to implement the proposed filter. This approach is useful to enhance the system performance by taking optimal advantage of embedded Multipliers, BRAMs and Registers available on target FPGA. The proposed design is implemented in a fully parallel fully pipelined style by taking optimal advantage of embedded Multipliers, Block RAMs and Registers available on target device.

IV. System Design

The proposed 2D filter is designed using Mat lab and Xilinx DSP Tools, synthesized with ISE 10.1 and implemented on Virtex-II Pro based 2vp50ff1148-7 FPGA device. Results show enhanced performance of proposed design in terms of area utilization as compared to standard optimal median filters.

The FPGA implementation provides the necessary performance for real-time image and video processing, while retaining the system flexibility to support an adaptive algorithm. The 5x5 size mask is used to implement the filter. The 2-D filter coefficients are stored in a block RAM and 5 MAC units are used to implement the proposed design in fully parallel and fully pipelined manner. The optimized VHDL code is developed and synthesized using ISE 10.1i and implemented on Virtex target device.

Edge detection is a fundamental tool used in most image processing applications to obtain information from the frames as a precursor step to feature extraction and object segmentation. This process detects outlines of an object and boundaries between objects and the background in the image. An edge-detection filter can also be used to improve the appearance of blurred or anti-aliased video streams.

The basic edge-detection operator is a matrix area gradient operation that determines the level of variance between different pixels. The edge-detection operator is calculated by forming a matrix centered on a pixel chosen as the center of the matrix area. If the value of this matrix area is above a given threshold, then the middle pixel is classified as an edge.

This proposed edge detection design has been developed using a 2-D Image filter as shown in Fig1. It can be realized efficiently using n-tap MAC FIR Filters. The 5x5 size mask is used to implement the filter. The 2-D filter coefficients are stored in a block RAM and 5 MAC units are used to implement the proposed design in fully parallel and fully pipelined manner.

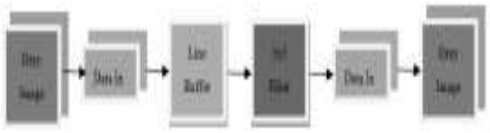

Fig.1 Proposed Edge Detection Model

The first step in design flow is to design 5-tap FIR filter using Simulink and System Generator as shown in Fig.2 Then the optimized VHDL code is developed and synthesized using ISE 10.1i and implemented on Virtex target device.

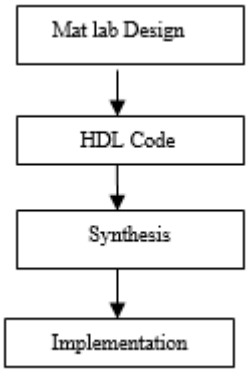

Fig.2 Proposed Design Flow

The incoming pixels are shifted through the line buffers that create a delay line. The buffer depth depends on the number of pixels in each line of the frame. These delay lines feed the filter array simultaneously with pixels from all the relevant video lines. At each filter node, the pixel is multiplied with the appropriate filter coefficients.

The architecture of fully parallel pipelined MAC based design is shown in Fig.3 the MAC based fully parallel implementation uses one multiplier each to process all 5 coefficients in a single clock and pipelined registers are used to enhance the speed performance of the filter. The proposed adaptive edge detection filter is implemented on Virtex II Pro based 2vp50ff1148-7 target device.

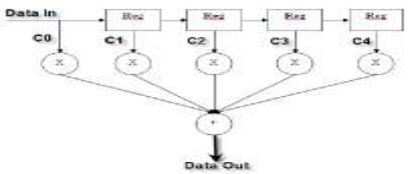

Fig.3 Fully Parallel MAC Architecture

V. Implementation & Results

The system implementation of the project starts by taking the gray image as input and converting it into text or binary input by using the Mat lab, and the filter is designed by Xilinx DSP Tools.

The proposed 2D filter is synthesized with ISE 10.1 and implemented on Virtex-II Pro based 2vp50ff1148-7 FPGA device. Results show enhanced performance of proposed design in terms of area utilization as compared to standard optimal median filters.

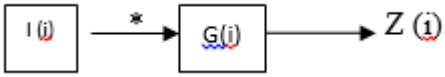

Fig4. Operation of Gaussian filter

$$I(i) = \begin{bmatrix} i0 & i1 & i2 \\ i3 & i4 & i5 \\ i6 & i7 & i8 \end{bmatrix}$$

$$Z(i) = \begin{bmatrix} 1 & 2 & 1 \\ 2 & 4 & 2 \\ 1 & 2 & 1 \end{bmatrix}$$

But the original input image is of 256*256 sizes at over all 774 pixel values is to be calculated the following equation.

$$Z=1/16 \sum g(i) * I(i)$$

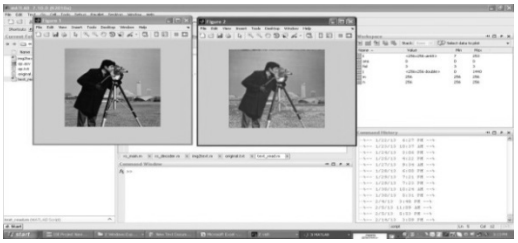

Fig 5 Mat Lab Filtering

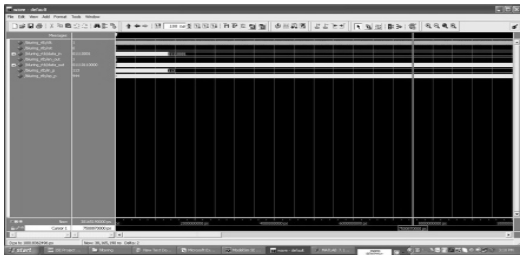

Fig6.Smoothening Simulation

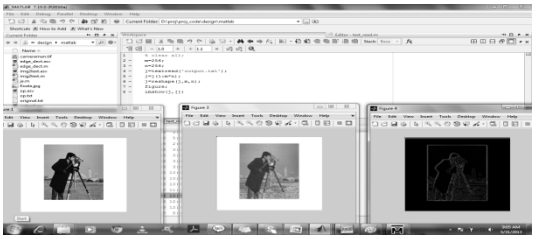

Fig7.Edge Detection

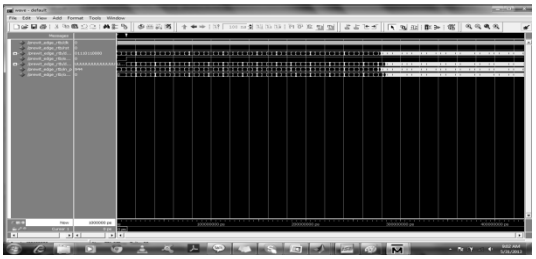

Fig8.Edge Detection Simulation Result

VI. Conclusion And Future Work

The proposed design consists of mat lab design for conversion of input image into text or binary followed by HDL design, The VHDL code for smoothening input image using Gaussian Filter is synthesized in Xilinx ISE12.2 .The code is simulated and analyzed by using ModelsimSE6.3f.

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