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CMOS MULTIPLIER DESIGN BASED ON ENHANCED COLUMN BYPASSING METHOD

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Abstract - This paper presents implementation of improved column bypassing scheme in a carry save multiplier architecture and do the comparative analysis with reference multiplier architectures. The multipliers are implemented in 130nm CMOS technology using LT spice simulation tool. The architectures are compared in terms of critical path delay, power dissipation and area in terms of transistor count. The power saving comes from bypassing signals along those adder columns in the array multiplier corresponding to zero bits in the multiplicand. Spurious signal switching activities can then be eliminated when bypassing occurs.

Keywords- multiplier, bypassing scheme

I. Introduction

Multiplication is fundamental operations in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore, low-power multiplier design has been an important part in low-power VLSI system design.

The basic array multiplier performs multiplication by arranging the full-adders to add the partial products for each output bit. However, this implementation uses a ripple-carry array that affects the delay. The second multiplier use bypassing scheme which addresses power consumption. In the second multiplier, bypassing scheme is implemented; that is full-adder is modified so that the full-adders can be turned off when not needed.

II. Review of Related Work

A. Array Multiplier

If we have two unsigned binary numbers Y =y n-1 y n-2 …y1 y0 and X = x n-1 x n-2 … x1 x0,the product P = YxX can be expressed as each partial product term of ai bj and can be evaluated using a two-input AND gate. All partial products therefore can be generated by an nxn array of two-input AND gates. The partial products can be summed by an n(n-1) array of 1-bit full adders. The arrangement is shown in Figure 1. The shifts implied by the terms 2i and 2j are implemented in the displacement of adders along the x and y direction

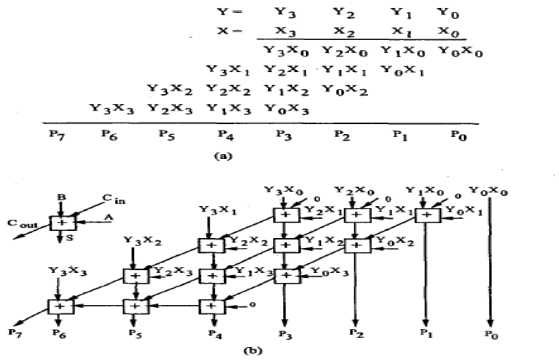

Fig 1. (a) Partial products of a 4x4 unsigned integer multiplication; (b) multiplier array

B. Low Power Multiplier with Bypassing and Carry save

This design combines two methods of optimization, bypassing and carry save. Bypassing disables an adder according to the multiplier bit. Since the adder is turned off, it will consume less power. The carry save structure optimizes for delay by shortening the

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critical path .Here output carry bits are passed diagonally downwards instead of only to the right we include an extra adder called a vector-merging adder to generate the final result.

The full-adder is modified to allow the bypass action. Two tri-state buffers controlled by the multiplier bit are added. At the output, a multiplexer will choose between the sum or the previous output depending on the value of the multiplier bit. Figure 2 shows the new full-adder cell. The modified FA cells are arranged similar to the array multiplier discussed in A. For an 4 x4 multiplier, the carry save structure is implemented by taking full adder Figure 3 shows the carry save structure Compared to the array multiplier, here the carry bits not immediately added, but rather are "saved" for the next adder stage, it has a advantage that its worst case critical path is shortened and uniquely defined.

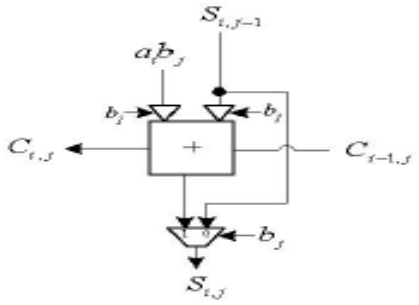

Fig. 2 . Modified Full-adder cell [2]

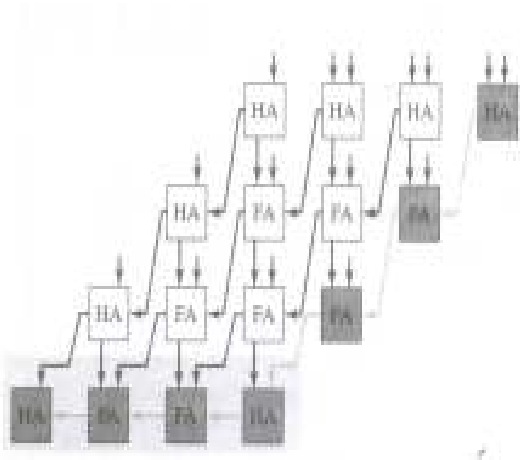

Fig 3. 4x4 carry –save multiplier

Bypassing is classified into two row and column bypassing.

C. Row bypassing

Bypassing with reference to multiplier means bypassing adders when its outputs are already known either in columns or rows or both in the multiplier array whenever certain multiplier or multiplicand or both bits are zero. The row bypassing technique is based on number of zeros in the multiplier bits .In this multiplier operation some of the rows of adders in the basic multiplier array inputs are tri state depending upon multiplier bits i.e whether Yj=1 or 0 (bypassed)) which will reduce power consumption as proposed in reference [6].Figure.4. shows the modified adder cell for row bypassing multiplier.

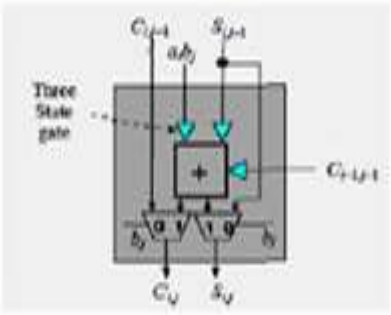

Fig. 4. Full adder cell for row bypassing

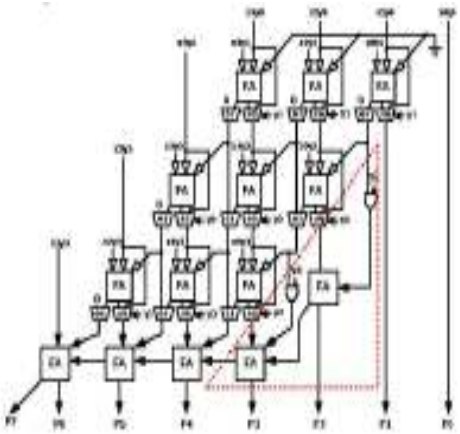

Fig 4.a Row bypass multiplier [6]

The schematic of a multiplier with row bypassing scheme is illustrated in Figure 4.a where y0,y1,y2 and y3 are multiplier bits. The input tri-state buffers serve as input gating when any of the multiplier bits are '0's and the multiplexers are used to select between the full adder output and already know input for a given FA in given row. The main drawback of this implementation is that tri state input control will fail due to leakage problem when working in low frequency. The degraded signals may cause both P and N logics turned on simultaneously and result in DC power dissipation.

D. Column bypassing

In this column bypassing the FA output in the respective column whose multiplicand bits (X0,X1,X2,X3) are '0's is bypassed with already known output, which reduces power consumption. This technique is totally dependent on number of zeros in the multiplicand bits ,unlike the row bypass multiplier .The advantage of the approach is the modified FA is simpler than that used in the row –bypassing multiplier .Following fig. 5 shows the modified FA cell for the column bypassing multiplier.

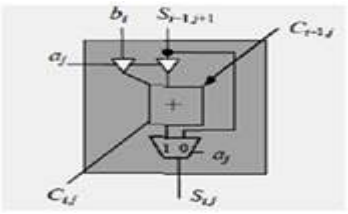

Fig.5 Full adder cell for column bypassing

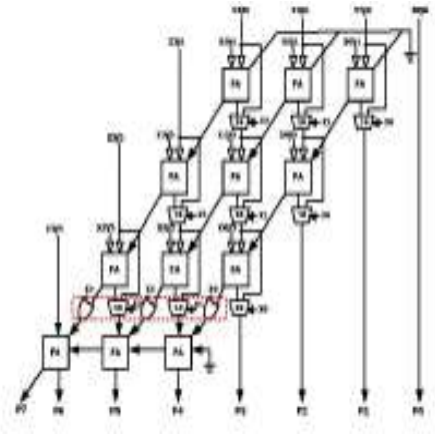

Fig 5.a column bypass multiplier [7]

multiplier schematic is given in Figure 5.a.here x0,x1,x2andx3 are multiplicand The idea comes from the observation that when a bit of the multiplicand is zero; as this is CSA based array carry will propagate down the column in diagonal, so the carry bit for given column whose multiplicand bit are '0's , 0 is propagated down in diagonal in the column; so all full adders along the corresponding diagonal (column) will have Cin=0 and summand inputs equal to zero (as Xi=0). The third input is then bypassed to the sum output. Since all Cout's along the diagonal are zeros, the Cin inputs to the carry propagation adder at the bottom of the array multiplier can be simply be gated to with Xi to have correct value.

The circuit overhead of the column bypassing scheme is smaller than that of the row bypassing scheme in that only one multiplexer per adder cell is needed (compared with the row bypassing scheme). In general, bypassing technique is a generic architecture design measure orthogonal to other low power schemes. It does not require elaborate transistor size tweaking as needed in other delay sensitive schemes. There is no need of extra clock signals and delay cells either. In this paper, we will devise an improved column bypassing scheme which will reduce both the

circuit and power overhead of the bypassing circuitry.

III. Low Power Multiplier Design Based On Improved Column Bypassing

Previous bypassing approaches are promising but some factors are overlooked. Tri-state buffers are used to retain or freeze data at input nodes during bypass. These data will degrade with time due to current leakage problem. When a sufficient voltage drop is reached, it leads to simultaneous operation of both P and N networks and thus means DC power consumption. The tri-state buffers and multiplexers also mean additional circuit overhead and the induced power consumption offsets the power saving through bypassing.

In this proposed design, the goal is to reduce the power the without degrading the input voltage levels. The cmos inverter and the transmission gate also serve as the 2-to-1 multiplexer for bypassing. The carry out signal is not guarded because the power saving is offset by the additional logic consumption and circuit overhead as well. To achieve bypass, two mechanisms must be used: signal multiplexing (using multiplexers) and evaluation suspension (using tri state buffers). In the design c2mos is used to serve both purposes. The basic idea is logic evaluation suspension instead of input signal retention or suspension. The tri-state buffers are removed and the full-adder design is replaced by the design in Figure 6. The logic is implemented in cmos and evaluation is guarded by a bypass signal to avoid the DC power consumption provided.

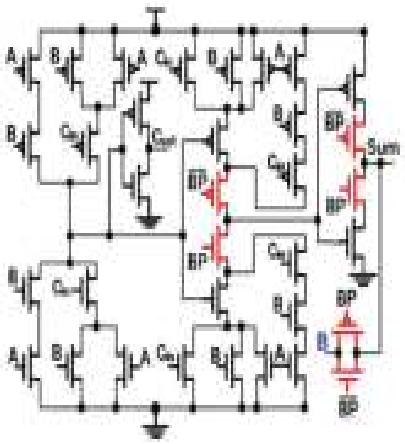

Fig 6 Design 1 cmos full adder design for column bypassing scheme

IV. Methodology

Each multiplier is implemented in 130nm CMOS technology using LT Spice circuit simulator. The blocks used are: two-input AND gate, full adders, tri-state buffer, and 2x1 multiplexer

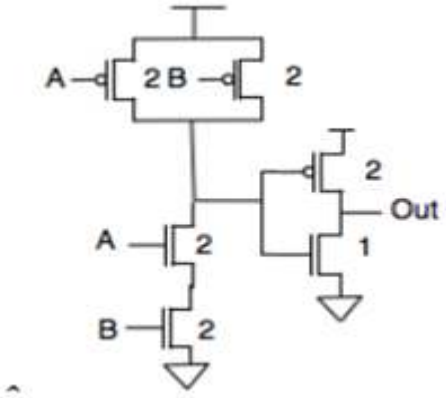

Fig 7. Two input AND gate

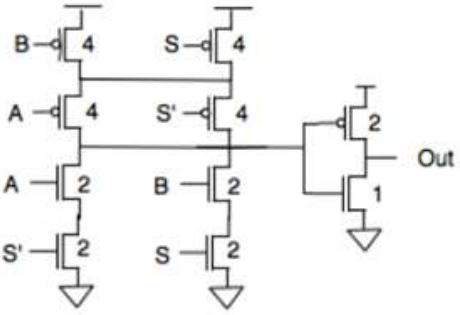

Fig 8. 2 x1 multiplexer

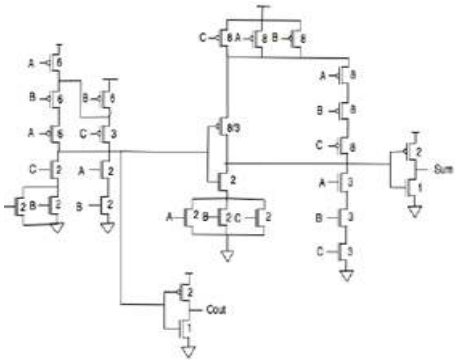

Fig 9. Full adder circuit

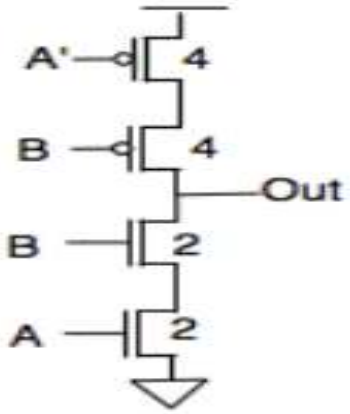

Fig 10. Tri-state buffer

Each multiplier architecture is implemented using the blocks previously mentioned. For each multiplier, a partial product generator block is needed. This is just an array of two-input AND gates that generate the partial products. The partial products are used in the full adder arrays of each multiplier.

@10Mhz	1.2v	1.5v	1.8v
Design 1	-15.2uW	-29.02uW	-54.4uW
Row [6]	-25.9uW	-54.4uW	-108uW
Column[7]	-26.4uW	-58uW	115uW

For the array multiplier, the full adder array arrangement in Figure 1 is implemented. For the bypassing multiplier with carry save, a modified full adder cell is used similar to Figure 6 This is where the tri-state buffer and multiplexers were used. Then an multiplier with bypass and carry save is implemented .

The multipliers are tested at V = 1.2, 1.5, and 1.8 V. The delay and power dissipation are measured.

V. Simulation Results and Comparisons

To evaluate the power saving merits the multiplier designs are implemented and simulated. These include the proposed two designs, one row bypassing design from [6], one column bypassing design from [7] plus the deign 1 which is the improved column bypassing The target technology is 130nm CMOS process A total of 4,000 test patterns are generated randomly with two probability settings, i.e. 50% or 75% of the operand bits being zero. The former setting is for the general applications where 0's and I's exhibit equal probability. The latter setting is for the cases most likely in fixed point DSP applications. The working frequency is set as 10MHz while the Vdd is scanned from 1.1V to 1.8V. Table I gives the results of 4X4multiplier designs with 50% of zero bit setting. (Negative number means power saving).

Table I

Power consumption saving of 4X4 bypassing scheme multiplier design with 50% zero probability

Here Design 1 have less power consumption compared to the other two .If the multiplier bits are increased we can see a large difference. Simulation waveform at 1.2v is given below

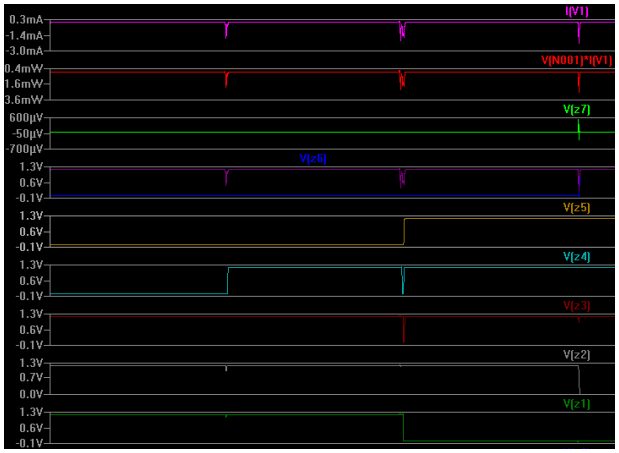

Fig 11. vdd current waveform of Design 1

For the Design 1 Figure 11 depicts the Vdd currents and power of Design I DC currents at design[1] is less compared of design [7] The situation becomes even worse under either low frequency or high voltage operations. The row bypassing design in [6] also suffers the same problem. Since its circuit overhead is larger than that of the column bypassing scheme, the power consumption overhead is even bigger.

Table II summarize the power saving performance of Design I, [7] and [6] configured in 4X4 array with 75% probability

Table II.

Power consumption saving of 4X4 bypassing scheme multiplier design with 75% zero probability

@10Mhz	1.2v	1.5	1.8
Design 1	-15uW	-29uW	-49uw
Row [6]	-39.3uW	-78.1uW	-273uW
Column[7]	-32.2uW	-65.07uW	-125uW

The performance of design 1 better when the multiplier size is increased. Since the 75% probability consists more number of 0 bits power saving should improve it can be seen if we are using more multiplier bits. In 75% probability desing1 performance is better compared to 50% probability.

We also analyze the circuit overheads of different bypassing schemes and the results are compiled into Table III. The analytical expressions of the transistor count for each logic module are presented. Note that in our designs, the bypassing logic is embedded in the adder cell. The incurred transistor account is thus added to that of the adder cell in base array. To give readers better understanding of the circuit complexity, the numbers for n = 4 are calculated. In this case, Design I enjoys the lowest circuit overhead. The circuit overhead next is the column[7] and last is row[6]. In VLSI, Digital circuits with less circuitry will have less switching activity that have less spurious signals, consumes less power. In our proposed design the transistor count is less when compared to design in Reference [6,7] and power consumption is less as mentioned above tables. The difference will be significant when we use our proposed scheme for 8x8, 16x16 bit multiplier designs.

Table III.

Transistor Count

	Transistor count When n=4
Array multiplier	336
Design 1	426
Row[6]	436
Column[7]	494

VI. Conclusion

In summary, in this paper we propose adder cell designs for the array multiplier using improved column bypassing scheme. Proposed designs

successfully integrate the bypassing logic and the adder cell into one which reduce the circuit overhead, delay also consumes very less power.

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