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A LOW NOISE TRIPLE PHASE SLEEP SIGNAL SLEW RATE MODULATION USED IN MTCMOS CIRCUITS

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Abstract--Triple phase Sleep signal slew rate modulation techniques for suppressing mode-transition noise are explored in this paper. A triple-phase sleep signal slew rate modulation (TPS) technique with a novel digital sleep signal generator is proposed. Reactivation time, mode-transition energy consumption, leakage power consumption, and layout area of different MTCMOS circuits are characterized under an equal-noise constraint. Influences of within-die and die-to-die parameter variations on the reactivation noise, time, and energy consumption of sleep signal slew rate modulated MTCMOS circuits are evaluated with a process imperfections aware robustness metric. The proposed triple-phase sleep signal slew rate modulation technique enhances the tolerance to process parameter fluctuations by up to 183.1× as compared to various alternative MTCMOS noise suppression techniques in a UMC 80-nm CMOS technology**.**

Keywords-low noise, mode transition energy, power and ground bouncing noise, process variations, reactivation time, sleep signal rise delay, triple-phase wake-up.

I. Introduction

MULTI-THRESHOLD CMOS (MTCMOS), also knownas power/ground gating, is the most commonly usedcircuit technique for leakage power reduction. Anintegrated circuit is typicallydivided into multiple autonomouspower/ground gating domains for effective reduction of leakage power consumption. When an idle circuitis awaken, high currents flow through the sleep transistors. Significant voltage fluctuations occur on the power and ground distribution networks (power and ground bouncing noise).Mode transition noise produced byan awakening circuit block propagates to the already active circuit blocks in the neighboring domains through the shared power and ground distribution networks. Logic states of internal nodes in surrounding active circuits are disturbed due to significant noise. Increasing numbers of (finer-grain) independently power/ground-gated logic and memory domains are employed for enhanced energy efficiency in modern integrated circuits. With more frequent transitions between the ACTIVE and SLEEP modes of operation to achieve more effective leakage power savings; reactivation noise has become an important reliability concern in modern integrated circuits Sleep signal slew rate modulation techniques are presented in this paper for suppressing the power and ground distribution network noise that are produced by MTCMOS circuits. Multi-phase sleep signal slew rate modulation techniques are investigated to mitigate noise while significantly reducing reactivation time and energy consumption in MTCMOS circuits. The reactivation time, mode transition energy consumption, leakage power consumption, and layout area of MTCMOS circuit techniques are characterized under an equal noise constraint. The impact of process variations on thereactivation noise, time, and energy consumption of MTCMOScircuits is also evaluated.This paper is organized as follows. An alternative triple-phase sleep signal slew rate modulation(TPS) technique is presented in Section II. A new fully digitaltriple-phase sleep signal generator is proposed. The previously published stepwiseVgs MTCMOS circuit technique isreviewed in Section III. Different design options are presentedin Section IV to modulate the slew rate of activation signals inMTCMOS circuits under an equal-noise constraint.

II. Triple-Phase Sleep Signal Slew Rate Modulation

A slowly rising sleep signal iseffective for suppressing the reactivation noise in MTCMOScircuits. A slowly rising sleep signal, however, also significantly increases the reactivationtime and energy consumptionof MTCMOS circuits. The single-phase sleep signal slewrate modulation technique is therefore not suitable for fastand energy efficient power/ground gating in high-performanceintegrated circuits.An alternative triple-phase sleep signal slew rate modulation (TPS) technique is presented in to suppress thereactivation noise while accelerating the reactivation processin MTCMOS circuits. The concept of TPS. As discussed in Section II, the sleep transistor producesnegligible noise in the weak inversion region of operation(when Vgs<Vthsleep). The sleep signal is preferred to risefaster from 0 V to the threshold voltage of sleep transistor inorder to reduce the overall reactivation time without producingsignificant noise. Reactivation noise is primarily produced afterthe sleep transistor is turned on. The sleep signal should betherefore subsequently decelerated as the gate voltage levelreaches the threshold voltage of sleep transistor. Decelerationof sleep signal suppresses the peak mode transition noise thatis produced after the sleep transistor is fully activated.After the VGND voltage is reduced to a very low

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levelclose to 0 V (time pointTB asshowninFig.4),themodetransition noise diminishes to a negligibly low level. The riseof sleep signal should therefore beagain accelerated to shortenthe remaining duration of reactivation process. Due to theshorter periods of Phase_1 and Phase_3, the reactivation timeand energy consumption of MTCMOS circuits are reducedwith the TPS technique as compared with the single-phasesleep signal slew rate modulation technique that is presentedin Section II.A mixed-signal switched capacitor circuit is proposed fortriple-phase sleep signal slew rate modulation in. Themixed-signal sleep signal modulator is shown in Fig. 1. TheVgs of sleep transistor is increased with small voltage steps.Additional clock signal and voltage bias sources (Vbias1,Vbias2, and Vbias3) are required for the operation of thismixed-signal circuit. Complex analog circuitry is employedto produce the three phases of sleep transistor activation.The mixed-signal sleep signal modulator consumes significantpower and occupies a large layout area. The rising speedof sleep signal cannot be tuned individually during Phase_1and Phase_2 with the sleep signal modulator that is describedin Phase_1 is inevitably elongated together with Phase_2to suppress the reactivation noise. The triple-phase reactivationtime reduction that is achievable with this mixed-signal sleepsignal generator is therefore limited. Furthermore, the sleepsignal slew rates during Phase_1 and Phase_2 strongly dependon the value ofCpump[see Fig. 1(a)]. Variations ofCpumpdueto process fluctuations significantly degrade the effectivenessof this mixed-signal modulator for noise suppression.A digital circuit is presented in for triple-phase sleepsignal slew rate modulation. The sleep signal modulator inis effective for reducing the reactivation noise, time, andenergy consumption of MTCMOS circuits as compared tothe single-phase sleep signal slew rate modulation technique.The deactivation process (ACTIVE to SLEEP mode transition)with this digital sleep signal modulator is, however, overlooked in. During a deactivation event, high short-circuitcurrents are produced by the digital sleep signal modulator,thereby causing a significant amount of energy consumption.A new superior fully digital triple-phase sleep signal slewrate modulator is proposed in this paper. The circuit is shownin Fig. 6. Sleep Global is the input signal of the new sleep signal modulator. Sleep Global triggers the activation and deactivation procedures of an MTCMOS circuit block. Sleep Localis produced by the proposed signal modulator and applied tothe gate terminal of the sleep transistor that controls the groundconnection of a local circuit.1.P1, P2,andP3are used for tuning the slew rate of Sleep Local duringreactivation events that occur in three phases.The new triple-phase sleep signal slew rate modulator operates as follows. In SLEEP mode, Sleep Globalis “0.” P1, P2,andP3 are cut off. Ndischarge is turned on.Sleep Local is maintained at~0 V. The sleep transistor is cut off. EN1 is maintained atVDDbyPreset1 that isturned on in SLEEP mode.Sleep Global transitions from “0” toVDDto initiate a reactivation event. PH1 transitions to low.P1is turned on to start thefirst phase (Phase_1) of reactivation. Sleep Local starts to rise.When Sleep Local reaches the threshold voltage ofNsenseL(low-|Vth|), NsenseL is turned on. EN1 is discharged throughNreset1 andNsenseL. PH1 transitions to high. P1is cut off. PH2transitions to low. P2 is thereby turned on to start the secondphase (Phase_2) of reactivation, where the sleep signal slew

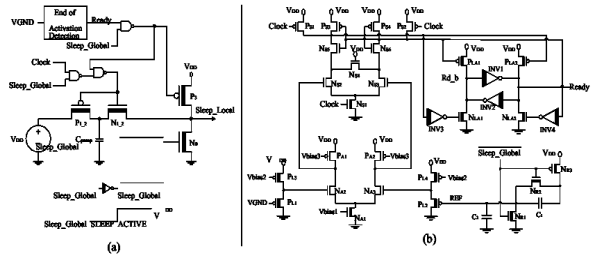

Fig.1. Schematic of the previously published mixed-signal triple-phase sleep signal slew rate modulator (TPS old). “Virtualground line of the ground-gated MTCMOS circuit. High-|Vth| transistors and CMOS logic gates are represented with thick lines in the transistor and gatesymbols, respectively. (a) Circuit structure of TPS old. (b) Schematic of the “end of activation detection” circuit block.

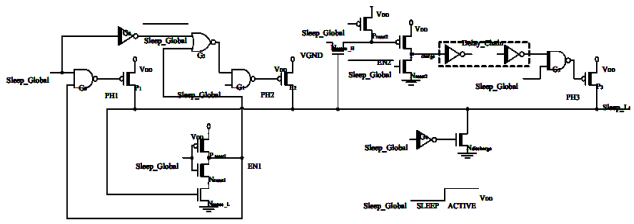

Fig.2. Schematic of the new fully digital triple-phase sleep signal slew rate modulator. “Sleep Global” is the input signal coming from the on-chip powermanagement unit. Rate is reduced. The VGND is discharged primarily duringPhase_2. Highest switching currents are produced in this phaseas the internal nodes in the awakening low-|Vth| circuit blocktransition to correct logic states. The rise of Sleep Local isintentionally decelerated by turning onP2while cutting offP1in Phase_2. P2 is designed (sized) to be significantly weakeras compared to P1. The peak reactivation noise produced byan awakening MTCMOS circuit is thereby mitigated.When the VGND is discharged to a relatively low voltagelevel, the voltage difference between Sleep Local and VGNDbecomes higher than the threshold voltage ofN sense H (high-|Vth|). N sense H is turned on. EN2 (maintained at VDD inSLEEP mode) is discharged Pcharge is activated. After thedelay of “Delay Chain” andG5, PH3 transitions to low. P3is turned on to start the third phase (Phase_3) of reactivation where the rate of

change of Sleep Local is increasedagain. Weak P2 is maintained on to assist the significantlystronger P3 as Sleep Local is raised faster toward VDDinPhase_3.During a deactivation event, Sleep Global transitions fromVDDto "0." PH1, PH2, and PH3 transition to high after thedelay ofG0, G1 andG5, respectively. P1, P2,andP3 arecut off. AlternativelyNdischargeis turned on after the delay ofG4. Sleep Local is discharged to ~0VbyNdischarge, therebydeactivating the MTCMOS circuit. SinceP1, P2,andP3 aredisabled beforeNdischargeis turned on, no short-circuit currentis produced by P1, P2,andP3 in this new digital sleepsignal modulator.

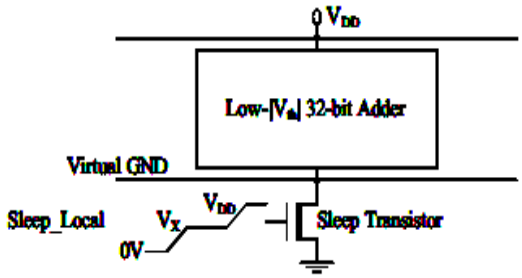

Fig.3. Illustration of the stepwiseVgs MTCMOS circuit technique .High-|Vth| sleep transistor is represented with a thick line in the channelarea.

With the triple-phase sleep signal slew rate modulatorthat is shown in Fig. 6, the rising speed of sleep signalis adjusted by monitoring the voltage level of Sleep Localand VGND. The transitions between the three phases ofreactivation occur automatically. No additional control signalsor voltage bias sources are required by the new sleep signalslew rate modulator. Furthermore, the proposed sleep signalmodulator is a digital circuit with lower power consumption,smaller area, and enhanced immunity to process variations ascompared to the mixed-signal sleep signal modulator circuitthat is presented in.Although the triple-phase sleep signal slew rate modulation idea is discussed in, the effectiveness of the TPStechnique for suppressing mode transition noise and reducingreactivation delay is not quantitatively evaluated in Threeimplementations of the TPS technique with the previouslypublished mixed-signal sleep signal slew rate modulator, thedigital sleep signal modulator that is presented in, and thenew digital sleep signal modulator that is shown in Fig. 6 arecharacterized in the following sections of this paper.

III. Step WiseVgs MTCMOS

The previously published [7] stepwise Vgs MTCMOS circuit technique to suppress mode transition noise is reviewed in this section. The stepwise Vgs MTCMOS circuit technique is illustrated in Fig. 7. The slew rate modulation technique is also applied to the stepwise Vgs MTCMOS circuit in this paper. The slew rate modulated stepwise Vgs MTCMOS circuit is evaluated in the subsequent sections. A stepwise Vgs MTCMOS circuit is activated in two steps as follows. The sleep signal transitions from 0 V to an intermediate voltage level VX (0 V < VX < VDD) during the first step of a reactivation event. The sleep transistor is weakly activated with a low gate voltage (VX). Although the voltage swing on the VGND is relatively high during the first wake up step, the amplitude of the first noise waveform is suppressed due to the weak conductivity of the sleep transistor. After the VGND is discharged to a sufficiently low voltage level, the sleep signal transitions from VX to VDD. The sleep transistor is strongly turned on. VGND is discharged to ~0 V following the full activation of the sleep transistor (Sleep_Local = VDD). The amplitude of the second noise waveform is also suppressed due to the lower voltage swing on the VGND during the second wake up step.

A Sleep signal modulator for stepwise Vgs MTCMOS circuit is presented in [8]. The circuit is shown in Fig. 8. During the

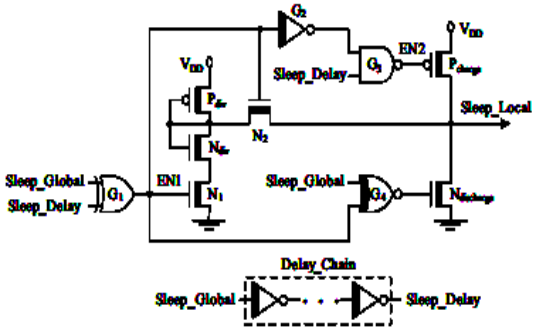

Fig.4. Schematic of the sleep signal modulator for stepwiseVgsMTCMOScircuit. "Sleep Global" is the input signal coming from the on-chippower management unit.

"Sleep Local" is the sleep signal applied to thelocal ground-gated MTCMOS circuit block. High-|Vth|transistors and CMOSlogic gates are represented with thick lines in the transistor and gate symbols,respectively.

First wake up step, N2 is turned on. Pdiv and N2 raise Sleep_Local from 0 V to VX. The value of VX is determined by the voltage divider that is composed of the diode-connected pMOS transistor Pdiv, diode-connected nMOS transistor Ndiv, and N1. During the second wake up step, N2 is cut off, while Pcharge is activated. Sleep_Local is raised from VX to VDD by Pcharge. While the stepwise Vgs is a potentially effective technique for mode transition noise suppression, many practical design challenges of stepwise Vgs MTCMOS circuits are over-looked in . The methodology needed to choose an appropriate intermediate voltage VX is not provided. The influence of sleep signal slew rate on reactivation noise is not discussed. The

optimum VX that minimizes the peak reactivation noise varies with the threshold voltage of sleep transistor. The effectiveness of stepwise Vgs in suppressing reactivation noise is therefore strongly affected by process variations. Parameter fluctuations and other implementation challenges of stepwise Vgs MTCMOS circuits are discussed in detail in the following sections of this paper.

IV.SleepSignalSlewrateModulationTechniques Underequal-NoiseConstraint

Single-phase sleep signal slew rate modulation, triple-phasesleep signal slew rate modulation, and stepwiseVgsMTCMOScircuit techniques are evaluated in this section under an equalnoise constraint. The sleep signal waveforms are tuned to suppress the peak ground bouncing noise to a negligible level thatis less than 2 mV with different MTCMOS circuit techniques.Peak noise voltages that are less than 2 mV are considered tobe negligibly small in this paper. The reactivation delay andenergy consumption of MTCMOS circuits are evaluated withthis noise criterion. The Reactivation DelayisReactivation Delay=Max{Ground Stability Delay, Sleep Local Delay}(1)where Ground Stability Delay is the time interval from Sleep Local rises to 10 mV until the virtual ground voltage

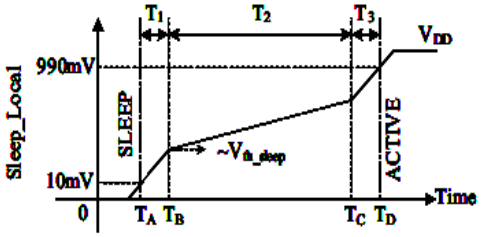

Fig.5.Timing diagram of the local sleep signal with the TPS MTCMOScircuit.

Stabilizes below 10mV.Sleep_Local_Delay is the time interval from Sleep_Local rises to 10 mV until Sleep_Local stabilizes above 990 mV.

A. Single-Phase Sleep Signal Slew Rate Modulation

The design of single-phase sleep signal slew rate modulated MTCMOS circuit is briefly described in this section. In order to satisfy the maximum acceptable ground bouncing noise criterion of 2 mV, the rise delay of single-phase sleep signal (Sleep_Local_Delay) needs to be at least 43.40 ns.

The sleep signal slew rate modulator for the single-phase sleep signal slew rate modulated MTCMOS circuit is composed of two inverters. The rise delay of the single-phase sleep signal is modulated by tuning the size of the pull-up transistor (Psingle_charge) in the second-stage inverter of the sleep signal slew rate modulator.

B. Triple-Phase Sleep Signal Slew Rate Modulation

The design of TPS MTCMOS circuit to satisfy the equal noise constraint is presented in this section. The timing diagram of the local sleep signal with the TPS MTCMOS circuit is illustrated in Fig. 9. At TA, Sleep_Local reaches 10mV. PH2 is discharged to VDD/2 (halfway through the high-to-low transition voltage swing) and P2 is effectively turned on at TB. The delay of the feedback loop (composed of Nreset1, Nsense_L, and G0 in Fig. 6) is tuned to ensure that P1 is cut off by the time Sleep_Local rises to the threshold voltage of sleep transistor (VSleep_Local = ~Vth_sleep =~370 mV [23]). Duration of Phase_1 (T1) is the time interval from TA to TB. By adjusting the delay of the feedback loop composed of Nsense_H, Pcharge, “Delay_Chain” (in Fig. 6), and G5, P3 is activated after the VGND is discharged to 10 mV. PH3 is discharged to VDD/2 (halfway through the high-to-low transition voltage swing) and P3is effectively turned on at TC. Duration of Phase_2 (T2) is the time interval from TB to TC. At TD, Sleep_Local rises to 990 mV. Duration of Phase_3(T3) is the time interval from TC to TD.

The values of T1 and T2 are tuned to suppress the peak ground bouncing noise to a negligible level below 2 mV. Furthermore, T1 is modulated to minimize the energy delay product (EDP) during the first two phases of reactivation. The EDP is

EDP = Phase1+2 Energy × Phase1+2 Delay (2)

Where Phase1+2 Delay is the duration of Phase_1 and Phase_2 (T1 + T2). Phase1+2 Energy is the total energy consumed by

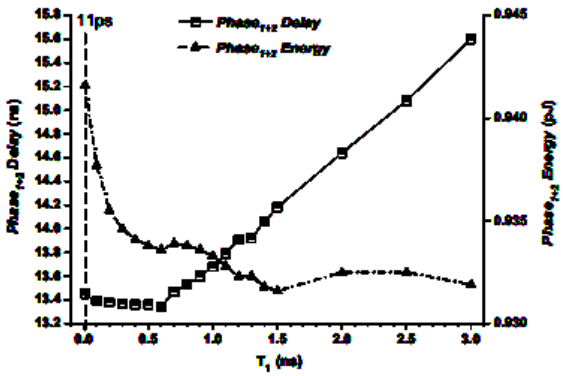

Fig.6. Phase1+2 Delay and Phase1+2 Energy of TPS MTCMOS circuit for different durations of Phase_1. T1 is varied from 11 ps to 3 ns. 11 ps is approximately the minimum achievable 10 to 370 mV rise delay in this UMC 80-nm CMOS technology.

The MTCMOS circuit during Phase_1 and Phase_2. When T1 is relatively small (T1 < 600 ps), the noise produced during Phase_1 affects the subsequent Phase_2 noise. For these relatively short durations of Phase_1 (T1 < 600 ps), decreasing T1 requires an increase in T2 to be

able to satisfy the maximum acceptable noise criterion of 2 mV. The overall Phase1+2 Delay is thereby increased with reduced T1for T1 < 600ps as shown in Fig. 10. Alternatively, when T1 is relatively large (T1 > 600ps), the influence of noise produced during Phase_1 is small on Phase_2 noise. The duration ofPhase_2 that is required to satisfy the equal-noise constraint is therefore maintained approximately constant (T2 variation less than 1.5%) for 600 ps< T1 < 3 ns. Phase1+2 Delay is increased approximately linearly with T1 for T1 > 600 ps as shown in Fig. 10. The minimum Phase1+2 Delay is observed when T1 is 600 ps. The voltage swings of the VGND and the internal nodes of low-|Vth| 32-bit adder are similar during T1 and T2. When T1 is increased, the variation of Phase1+2 Energy is therefore negligible (less than 1.06% variation as T1 is increased from

11ps to 3 ns) as shown in Fig. 10. Similar to the minimum Phase1+2 Delay, the minimum EDP is also observed when T1 is 600ps as shown in Fig. 11. For this optimum duration of Phase_1 (T1 = 600 ps), T2 needs to be at least 12.75 ns to satisfy the peak acceptable ground bouncing noise criterion of 2 mV. At the end of Phase_2, the sleep signal rises to 636 mV and the VGND is discharged to 10 mV.

The reactivation noise is primarily produced during Phase_2. The duration of Phase_3 (T3) has no significant influence on the peak ground bouncing noise. T3, however, affects the energy consumption and delay of a reactivation event. Duration of Phase_3 (T3) is therefore important and tuned to lower the Reactivation EDP (REDP). The REDP is

REDP = Wake_Up_Energy×Reactivation_Delay (3)

Where Wake_Up_Energy is the total energy consumed by the MTCMOS circuit during the period of Reactivation_Delay. The Reactivation_Delay is defined in (1). The Reactivation_ Delay and Wake_Up_Energy of the MTCMOScircuit are monotonically increased with a longer T3 as shown in Fig. 12. The REDP therefore monotonically increases with longer

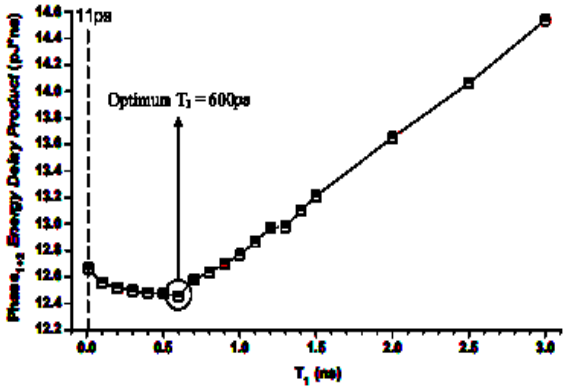

Fig.7. EDPof the first two phases of reactivation with the TPS MTCMOS circuit.T1is varied from 11ps to 3 ns.

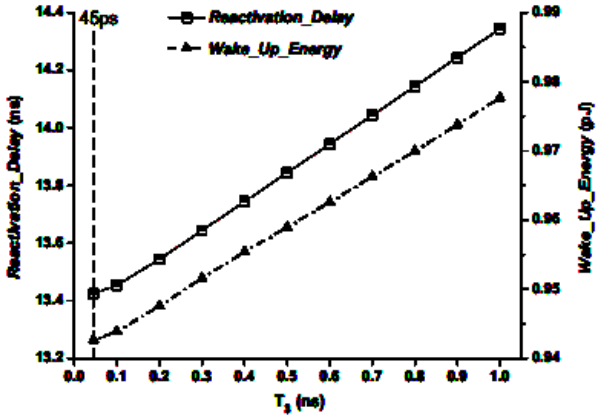

Fig.8. Reactivation Delay and Wake up Energy of TPS MTCMOS circuit for different durations of Phase_3. T3 is varied from 45ps to 1ns. 45ps is approximately the minimum achievable 636 to 990 mV rise delay in this UMC 80-nm CMOS technology.

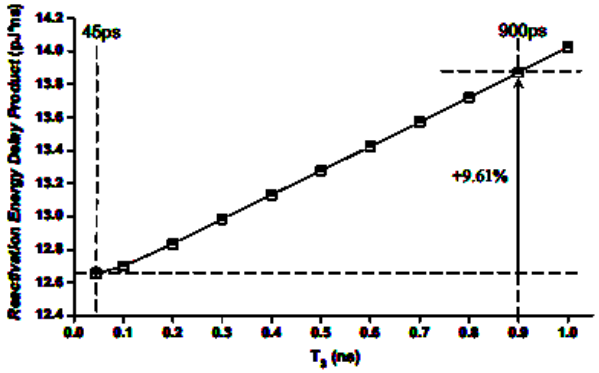

Fig.9. RED Pof TPS MTCMOS circuit for different durations of Phase_3.T3is varied from 45ps to 1ns.

T3 as shown in Fig.13. Minimum REDP is observed with T3=45 ps. To be able to realize the design option that requires the shortest possible Phase_3 duration of 45ps, P3 (in the triple phase sleep signal slew rate modulator that is shown in Fig. 6) has to be a very wide low-|Vth | transistor (width of P3 is

Table I
Parameters For Achieving Equal Noise With Sleep Signal Slew Rate Modulation Techniques

Circuit technique	Critical parameters
Single-phase	Rise delay of sleep signal: 43.40 ns.
TPS	T_1: 600 ps; T_2: 12.75 ns; T_3: 900 ps.
Stepwise V_{gs}	V_X: 0.49 V; T_{R_first}: 1.9 ns; T_{R_second}: 1.1 ns; T_{relax}: 10.76 ns.

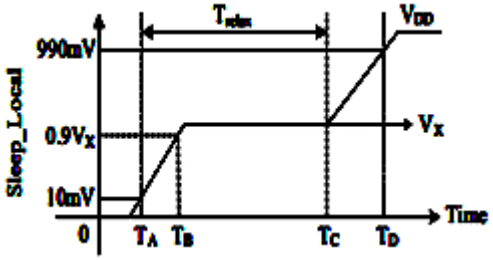

Fig.10. Timing diagram of the local sleep signal with the step wise Vgs MTCMOS circuit.

14.5μm) [6].High instantaneous currents are produced by the large P3 when Phase_3 is initiated during a wake-up event. Significant amount of additional switching noise is therefore produced and injected onto the ground distribution network by the triple-phase sleep signal modulator. The equal noise constraint is actually violated when the sleep signal modulator noise is included in the analysis (T3 = 45 ps) [6]. Due to the high noise produced by the sleep signal slew rate modulator, the power and ground distribution networks are further disturbed, thereby delaying the reactivation of TPS MTCMOScircuit as well [see the definition of Reactivation_Delay in (1)].Furthermore, higher leakage power and layout area overhead are caused by the sleep signal modulator when P3 is sized large enough to minimize T3 [6]. In order to avoid the high overhead of the design option with T3 = 45 ps, an alternative TPS MTCMOS circuit with a longer Phase_3 (T3 = 900 ps) is preferred in this paper. As shown in Fig. 13, when T3 is increased from 45 to 900 ps, the REDP difference is less than 10%. The critical timing parameters of this preferred implementation of TPS are listed in Table I.

C. Sleep Signal Slew Rate Modulated StepwiseVgs MTCMOS Circuit

The optimization of sleep signal slew rate modulated step wise Vgs MTCMOS circuit to satisfy the equal-noise constraint is presented in this section. The timing diagram of the local sleep signal with the stepwise Vgs MTCMOS circuit is illus-trated in Fig. 14. The relaxation time (Trelax) of stepwise Vgs MTCMOS circuit is the time interval from Sleep_Local rises to 10 mV until the virtual ground voltage is discharged to the relaxation voltage (Vrelax). Vrelax is

Vrelax = Max{1.1 ∗Vstable, 10 mV}(4) where Vstable is the steady state VGND voltage of the MTCMOS circuit when Sleep_Local is VX.At TA, Sleep_Local reaches 10 mV. At TB, Sleep_Local rises to 0.9VX. Sleep_Local rise delay is the time interval from TA to TB during the first step of reactivation. The strength of

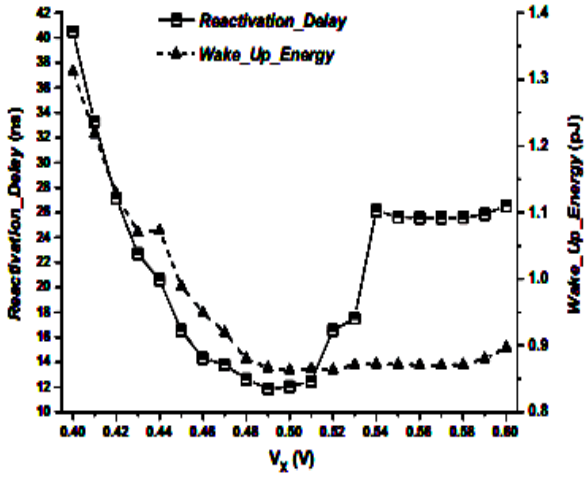

Fig.11.Reactivation_Delay and Wake_Up_Energy of sleep signal slew rate modulated stepwise Vgs MTCMOS circuit for different VX.

Pdiv and N2 (in Fig. 8) are tuned to ensure that Sleep_Local rises to 0.9VX at TB . By adjusting the delay of "Delay_Chain," G1, G2, and G3, Pcharge is activated after the VGND is discharged to Vrelax. EN2 is discharged to VDD/2 (halfway through the high-to-low transition voltage swing) and Pcharge is turned on at TC . Trelax is the time interval from TA to TC. At TD, Sleep_Local rises to 990 mV. Sleep_Local rise delay of the second step of reactivation is the time interval from TC to TD.

Sleep_Local rise delays of the two phases of reactivation are tuned to suppress the peak ground bouncing noise below 2 mV with the stepwise Vgs MTCMOS circuit. VX is optimized to minimize the REDP [defined in (3)]. For each value of VX , Sleep_Local rise delay (measured from 10 mV to 0.9VX) of the first step of reactivation is increased from the minimum achievable rise delay until the first wave of ground bouncing noise is suppressed below 2 mV. Afterwards, Sleep_Local rise delay (measured from VX to 990 mV) of thesecond step of reactivation is increased from the minimum achievable rise delay until the second noise waveform is also suppressed below 2 mV. Variations of the Reactivation_Delay [defined in (1)] and Wake_Up_Energy (defined in Section V-B) with VX are shown in Fig. 15.

When VX is relatively small (for example, 0.4 V), the VGND is discharged slowly by the weak sleep transistor during the first wake-up step. Furthermore, Sleep_Local rise delay of the second step of reactivation needs to be increased to suppress the peak amplitude of the second noise wave form below 2 mV. The Reactivation_Delay of stepwise Vgs MTCMOS circuit is thereby prolonged. Alternatively, when VX is relatively large (for example, 0.6 V), Sleep_Local rise delay of the

first step of reactivation needs to beelongated to suppress the peak amplitude of the first noise waveform below2 mV. The reactivation time is thereby also increased with a relatively large VX in a stepwise Vgs MTCMOS circuit. The minimum Reactivation_Delay is observed when VX is 0.49 V.

When VX is relatively small (for example, 0.4 V), the sleep transistor stays in the active region for a long time during the reactivation process. Significant leakage currents are produced by the low-|Vth| 32-bit adder. Furthermore, higher shortcircuit currents are produced during the reactivation process with small VX . Total Wake_Up_Energy of the stepwise Vgs MTCMOS circuit is thereby increased. As shown in Fig. 15, the Wake_Up_Energy of the stepwise Vgs MTCMOS circuit is significantly reduced (by 34.21%) when VX is increased from 0.4 to 0.5 V. The minimum Wake_Up_Energy is achieved when VX is 0.5 V. If VX is further increased beyond 0.5 V, the sleep transistor stays in the weak inversion region for a longer time during a reactivation event. The Wake_Up_Energy consumed due to leakage currents is thereby increased for VX > 0.5 V.

The REDP with different VX is shown in Fig. 16. Similar to the minimum Reactivation_Delay, the minimum REDP of stepwise Vgs MTCMOS circuit is also observed when VX is 0.49 V. The critical voltage and timing parameters of the stepwise Vgs MTCMOS circuit technique are listed in Table I.

V. Evaluation Of Sleep Signal Slew Rate Modulated Mtcmos Circuits

Four different sleep signal modulators are designed to produce the real sleep signals for the ground-gated MTCMOS circuits according to the parameters that are listed in Table I. Both the digital sleep signal modulator (TPS_A) that is presented in [6] and the new superior sleep signal modulator (TPS_B) that is shown in Fig. 6 are characterized in this section. The sizes of critical transistors are listed in Table II. Channel lengths of some of the transistors are longer than 2λ for suppressing the short-channel effects and providing enhanced tolerance to process variations.

A fifth mixed-signal triple-phase sleep signal slew rate modulator (TPS_old) is also designed and evaluated in this paper as shown in Fig. 5. The frequency of the clock signal that is required by TPS_old (see Fig. 5) is assumed to be 1-GHz. Cpump is selected (Cpump is implemented with a metal-oxide-semiconductor capacitor in the UMC 80-nm CMOS technology: Cpump=0.5fF) to limit the peak noise to approximately 2 mV during Phase_1 and Phase_2 of reactivation. P3 is sized (see Table II) to guarantee that the peak noise produced during Phase_3 is below 2 mV. The voltage at node "REF" [see Fig. 5(b)] is maintained at 10 mV. Phase_3 is thereby initiated when the VGND is

Table II
Critical Transistor sizes in different MTCMOS Circuits

Circuit technique	Critical transistor sizes
Single-phase	P_{single_charge}: $W = 120$ nm/$L = 2.06$ μm.
TPS_old [10]	P_{1_2}: $W = 160$ nm/$L = 160$ nm; N_{1_2}: $W = 160$ nm/$L = 160$ nm; P_3: $W = 600$ nm/$L = 160$ nm.
TPS_A [6]	P_1: $W = 160$ nm/$L = 160$ nm; P_2: $W = 120$ nm/$L = 2.16$ μm; P_3: $W = 780$ nm/$L = 160$ nm.
TPS_B (Fig. 6)	P_1: $W = 160$ nm/$L = 160$ nm; P_2: $W = 120$ nm/$L = 2.16$ μm; P_3: $W = 780$ nm/$L = 160$ nm.
Stepwise V_{gs} (Fig. 8)	P_{div}: $W = 180$ nm/$L = 160$ nm; N_{div}: $W = 160$ nm/$L = 160$ nm; P_{charge}: $W = 420$nm/$L = 160$ nm; N_1: $W = 160$ nm/$L = 160$ nm; N_2: $W = 240$ nm/$L = 160$ nm.

*UMC 80-nm CMOS technology. Minimum channel width = 120 nm. Minimum channel length = 80 nm.

Discharged to ~10 mV during a reactivation event. As illustrated in Fig. 5, high-|Vth| transistors are extensively employed in the mixed-signal sleep signal modulator to minimize the leakage power consumption. The voltage bias sources (Vbias1 = 0.48 V, Vbias2 = 0.5 V, and Vbias3 = 0.5 V)that are utilized in the mixed-signal sleep signal modulator are assumed to be available on-chip. The leakage power and area overhead of the voltage bias generators are not considered in this paper.

With the sleep signal generators in place, design tradeoffs among overall reactivation time, overall reactivation energy consumption, overall deactivation energy consumption, leak-age power consumption, and layout areas of MTCMOS cir-cuits are discussed in Section VI-A. The effects of process parameter variations on peak ground bouncing noise, overall reactivation time, and overall reactivation energy consumption of different MTCMOS circuits are evaluated in Section VI-B.

A. Characterization of MTCMOS Circuits

Various design metrics of MTCMOS circuits are characterized assuming the typical (nominal) process corner of UMC 80-nm CMOS technology in this section. The over- all reactivation time (TR), overall reactivation energy (ER), overall deactivation energy (ED), SLEEP mode leakage power consumption, and layout areas of different sleep signal slew rate modulated MTCMOS circuits are listed in Table III. The overall reactivation time (TR) is

TR =
Sleep_Signal_Modulator_DelayReactivation_Delay(5)

where the Sleep_Signal_Modulator_Delay is the time interval from Sleep_Global rises to 10 mV until Sleep_Local rises to10 mV. The Reactivation_ Delay is

defined in (1).The overall reactivation energy (ER) is the total energy consumed by a sleep signal modulator and MTCMOS circuit together during the overall reactivation time. The overall deactivation energy

(ED) is the total energy consumed by a sleep signal generator and MTCMOS circuit together during the deactivation delay (the time interval from Sleep_Global falls to 10 mV until Sleep_Local falls to 10 mV).

Various design metrics are compared among TPS_A, TPS_B, TPS_old, stepwise Vgs, and single-phase sleep signal slew rate modulated MTCMOS circuits next. As listed in Table III, the stepwise Vgs MTCMOS circuit reduces the overall reactivation time by 72.46%, 43.46%,16.09%, and15.92% as compared to the single-phase, TPS_old, TPS_A, and TPS_B MTCMOS circuits, respectively, when the fivecircuits are designed to produce similar ground bouncing noise. Due to the relatively shorter durations of Phase_1and Phase_3, TPS_B MTCMOS circuit reduces theover all reactivation time by 67.25% as compared to the single-phase MTCMOS circuit. The rising speed of sleep signal cannot be tuned individually during Phase_1 and Phase_2 with the mixed-signal triple-phase sleep signal slew ratemodulator that is presented in [9]. Phase_1 is therefore inevitably elongated together with Phase_2 to suppress the reactivation noise, thereby increasing the overall reactivation time as compared to the TPS_B MTCMOS circuit. TPS_B MTCMOS circuit reduces the overall reactivation time by 32.76% as compared to the TPS_old MTCMOS circuit.

The energy consumed during mode transitions is an important concern in MTCMOS circuits. Lower mode transition energy consumption enables an MTCMOS circuit to transition to SLEEP mode more frequently, thereby allowing more significant leakage power savings [16]-[19]. MTCMOS circuit techniques with suppressed mode transition energy consumption are therefore highly desirable. As listed in Table III, in addition to shortening the delay, TPS_A, TPS_B, andstepwiseVgs MTCMOS circuits also significantly lower the energy consumed during the reactivation events. Significant weak inversion currents are produced by the low-|Vth| 32-bit adder due to the longer reactivation process of the single phase MTCMOS circuit, thereby increasing the reactivation energy consumption by 1.93×, 1.92×, and 1.91× as compared to the stepwise Vgs, TPS_A, and TPS_B MTCMOS circuits, respectively. Due to the relatively longer reactivation time and the more complex and power hungry circuitry of the mixed- signal sleep signal modulator, the TPS_old MTCMOS circuit consumes 53.67%, 52.48%, and 52.33% higher energy as compared to the stepwise Vgs, TPS_A, and TPS_B MTCMOS circuits, respectively, during reactivation events.

During the deactivation process with the stepwise Vgs sleep signal modulator, Sleep_Local transitions from ~ VDD to an intermediate voltage level (between VDD and 0 V) before being fully discharged to ~0 V. Significant short-circuit currents are produced by Pdiv, Ndiv, and N1. The stepwise Vgs MTCMOS circuit therefore increases the deactivation energy consumption by 15.59×, 7.91×, and 6.71× as compared to the single-phase,TPS_B, and TPS_old MTCMOS circuits, respectively. Simi- larly, high short-circuit currents are produced by the TPS_A sleep signal modulator that is presented in [6], as discussed in Section III. The TPS_A MTCMOS circuit consumes 11.41×5.79×, and 4.91×higher energy as compared to the single- phase, TPS_B, and TPS_old MTCMOS circuits, respectively, during a deactivation event. The sleep signal modulator that is utilized for the single-phase MTCMOS technique is a simple circuit that is composed of two inverters. In the SLEEP mode where the sleep transistor

TABLE III
COMPREHENSIVE COMPARISON OF SLEEP SIGNAL SLEW RATE MODULATION TECHNIQUES

Circuit technique	Single-phase	TPS_old [10]	TPS_A [6]	TPS_B	Stepwise V_{gs}
Peak ground noise (mV)	2.090	2.197	1.810	1.999	2.337
T_R (ns)	44.12	21.49	14.48	14.45	12.15
E_R (pJ)	1.972	1.569	1.029	1.030	1.021
E_D (pJ)	0.034	0.079	0.388	0.067	0.530
SLEEP leakage power (nW)	70.0	342.2	86.0	87.1	87.2
Layout area (μm^2)	1505	1616	1550	1551	1573
Normalized *EQM*	2.10	1	7.16	9.15	7.58

is cut off (Sleep_Local = 0 V), the single-phase MTCMOS circuit reduces the leakage power consumption by 79.54%, 19.72%, 19.63%, and 18.60% due to the simpler and smaller sleep signal modulator as compared to the TPS_old, stepwise Vgs, TPS_B, and TPS_A MTCMOS circuits, respectively. Significant leakage currents are produced by the mixed-signal triple-phase sleep signal slew rate modulator (Vbias1 is gated low, while Vbias2, Vbias3, and clock are gated high in SLEEP mode). The TPS_old MTCMOS circuit that is proposed in [9] consumes 3.93× higher leakage power as compared to the newly proposed TPS_B MTCMOS circuit.

The single-phase MTCMOS circuit occupies the smallest silicon area. The single-phase MTCMOS circuit reduces the overall layout area by 6.87%, 4.32%, 2.97%, and 2.90% as compared with the TPS_old, stepwise Vgs, TPS_B, and TPS_A MTCMOS circuits, respectively.

In order to evaluate the overall quality of different sleep signal slew rate modulated MTCMOS circuits at the typical process corner, a comprehensive electrical quality

metric (EQM) is evaluated next. The EQM is

EQM= (TR ×(ER +ED)×Leakage_Power×Layout_Area)

Where Leakage_Power is the total leakage power consumed by a sleep signal modulator and MTCMOS circuit together in SLEEP mode (as listed in Table III). The normalized EQM (with respect to TPS_old MTCMOS circuit)is listed in Table III. The newly proposed TPS MTCMOS circuit (TPS_B) enhances the overall electrical quality by 9.15×, 4.35×, 1.28×, and 1.21× as compared to the old mixed-signal triple-phase [9], the single-phase, the previously proposed digital triple-phase (TPS_A), and thestepwise Vgs MTCMOS circuits, respectively. The newly proposed TPS MTCMOS is thereforeidentified as the most desirable mode transition technique in ground-gated integrated circuits at the typical process corner.

B. Influence of Process Variations

The fluctuations of process parameters alter the electricalcharacteristics of CMOS circuits [21], [22]. The effects of

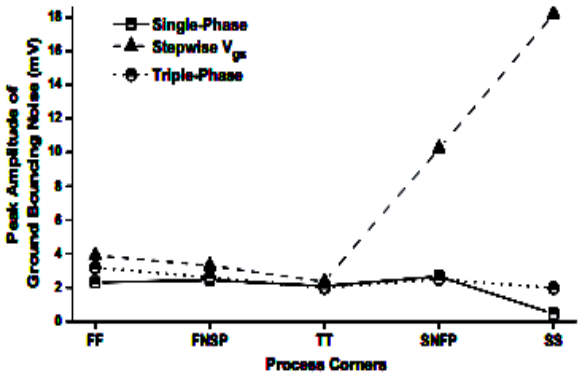

Fig. 12. Peak amplitudes of ground bouncing noise produced by sleep signal slew rate modulated MTCMOS circuits at different process corners.

Process variations on the peak ground bouncing noise, overall reactivation time, and overall reactivation energy consumption of sleep signal slew rate modulated MTCMOS circuits are evaluated in this section. The five process corners (TT: typical, FF: fast nMOS fast pMOS, FNSP: fast nMOS slow pMOS, SNFP: slow nMOS fast pMOS, and SS: slow nMOS slow pMOS) and the Monte Carlo model cards provided by the UMC 80-nm CMOS technology are used to evaluate the influence of die-to-die and within-die process variations, respectively, on MTCMOS circuits. The TPS MTCMOS circuits that are proposed in [6] and [9] are inferior to the other multiphase sleep signal slew rate modulation techniques that are evaluated in this paper even at the typical process corner. Furthermore, the additional clock signals and voltage bias sources cause significant design complexity and challenge with the mixed-signal triple-phase sleep signal slew rate modulator that is presented in [9]. Therefore, the previously publishedTPS MTCMOS circuits (TPS_old and TPS_A) are not further evaluated in this paper.

The peak amplitudes of ground bouncing noise produced by sleep signal slew rate modulated MTCMOS circuits at different process corners are shown in Fig. 17. The strength of nMOS transistors are degraded at the SNFP and SS process corners. The parasitic capacitors attached to the internal nodes of low-|Vth| circuit block and the VGND are not discharged to sufficiently low voltage levels at the end of the relaxation period (TC in Fig. 14) With the stepwise Vgs MTCMOS circuit. When the second wake up step is initiated, therefore, significant amount of noise is produced by the stepwise Vgs MTCMOS circuit as shown in Fig. 17.

The sensitivity of reactivation noise to die-to-die process variations is characterized next. The peak noise deviations of MTCMOS circuits are evaluated. The peak noise deviation (NDEV) is given in (7), shown at the bottom of the next page, where NFF, NFNSP, NTT, NSNFP, and NSS are the peak ground bouncing noise produced by MTCMOS circuits at the FF, FNSP, typical, SNFP, and SS process corners, respectively. As listed in Table IV, the triple-phase sleep signal slew rate modulated MTCMOS circuit reduces the peak noise deviation by 92.03% and 20.22% as compared to the stepwise Vgs and single-phase sleep signal slew rate modulated MTCMOS circuits, respectively. Fully digital TPS MTCMOS circuit

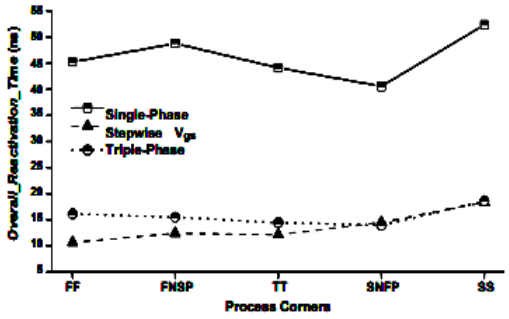

Fig.13.Overall reactivation times of sleep signal slew rate modulated MTCMOS circuits at different process corners.

Technique thereby maintains effectiveness for mode transition noise suppression across various process corners and offers the highest immunity to die-to-die process parameter fluctuations.

The overall reactivation time (TR) and overall reactivation energy (ER) of sleep signal slew rate modulated MTCMOS circuits at different process corners are shown in Figs. 18 and 19, respectively. In order to characterize the sensitivity of TR and ER of MTCMOS circuits to die-to-die process variations, the reactivation

time deviation and reactivation energy deviation of MTCMOS circuits with respect to the TR and ER at the typical process corner are evaluated. Reactivation time deviation (TR_DEV) and reactivation energy deviation (ER_DEV) are given in (8) and (9), shown at the bottom of the page, respectively.

As listed in Table IV, the TPS MTCMOS circuit achieves the lowest reactivation time deviation. The TPS MTCMOS circuit reduces TR_DEV by 54.72% and 32.55% as compared to the single-phase and stepwise Vgs MTCMOS circuits, respectively. Alternatively, stepwise Vgs MTCMOS circuit displays the lowest reactivation energy deviation. Stepwise Vgs MTCMOS circuit reduces ER_DEV by 82.91% and 37.21% as compared to the single-phase and triple-phase MTCMOS circuits, respectively.Next, the MTCMOS sleepsignal slew rate modulation techniques are compared under within-die process variations. 1000 Monte Carlo simulations are run to evaluate the statistics for peak ground bouncing noise, overall reactivation time, and overall reactivation energy consumption of different MTCMOS circuits. The Monte Carlo SPICE model cards provided by UMC are used for the simulations. The UMC 80-nm CMOS technology Monte Carlo SPICE model cards arebased on real wafer measurements [23]. Threshold voltage,

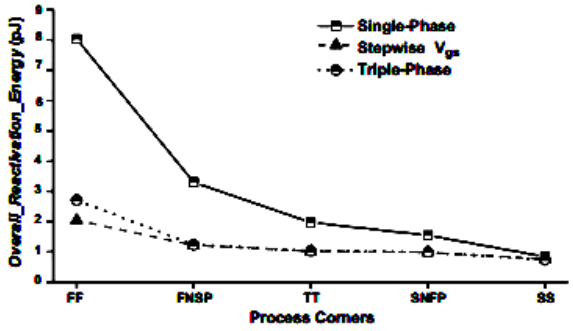

Fig.14. Overall reactivation energy consumptions of sleep signal slew rate modulated MTCMOS circuits at different process corners.

Table IV

Comprehensive Compariso MTCMOS Circuit Techniquesunder Process Variations

Circuit technique	Single-phase	Triple-phase	Stepwise V_{gs}
N_{DEV} (mV)	0.89	0.71	8.91
T_{R_DEV} (ns)	5.08	2.30	3.41
E_{R_DEV} (pJ)	3.16	0.86	0.54
N_{SD} (mV)	0.81	0.32	1.36
T_{R_SD} (ns)	1.77	0.90	0.91
E_{R_SD} (pJ)	0.47	0.13	0.14
Normalized *PIARM*	1	183.10	3.39

gate oxide thickness, carrier mobility, and channel doping concentration related parameters are assumed to have Gaussian distributions in the Monte Carlo SPICE model cards. The statistics for the peak ground bouncing noise, overall reactivation time, and overall reactivation energy consumption of MTCMOS circuits are illustrated in Figs. 20-22, respectively. The standard deviations of peak ground bouncing noise (N_{SD}), overall reactivation time(T_{R_SD}), and overall reactivation energy consumption (E_{R_SD}) are listed in Table IV.

The proposed digital triple-phase sleep signal slew rate modulator has the capability to initiate different phases of a reactivation process by monitoring the voltage levels of Sleep_Localand VGND. Triple-phase MTCMOS circuit thereby displays the smallest standard deviations of peak ground bouncing noise, overall reactivation time, and overall reactivation energy consumption under within-die process variations as listed in Table IV. Triple-phase MTCMOS circuit reduces the standard deviations of peak ground bouncing noise, overall reactivation time, and overall reactivation energy consumption by up to76.47%, 49.15%, and 72.34%, respectively, as compared to the other MTCMOS circuits

$$N_{SD} = \sqrt{\frac{(N_{SD} - N_{SD})^2 + (N_{SD(P)} - N_{SD})^2 + (N_{SD(PP)} - N_{SD})^2 + (N_{SD} - N_{SD})^2}{4}} \quad (7)$$

$$T_{R\_SD} = \sqrt{\frac{(T_{R\_SD} - T_{R\_SD})^2 + (T_{R\_SD(P)} - T_{R\_SD})^2 + (T_{R\_SD(PP)} - T_{R\_SD})^2 + (T_{R\_SD} - T_{R\_SD})^2}{4}} \quad (8)$$

$$E_{R\_SD} = \sqrt{\frac{(E_{R\_SD} - E_{R\_SD})^2 + (E_{R\_SD(P)} - E_{R\_SD})^2 + (E_{R\_SD(PP)} - E_{R\_SD})^2 + (E_{R\_SD} - E_{R\_SD})^2}{4}} \quad (9)$$

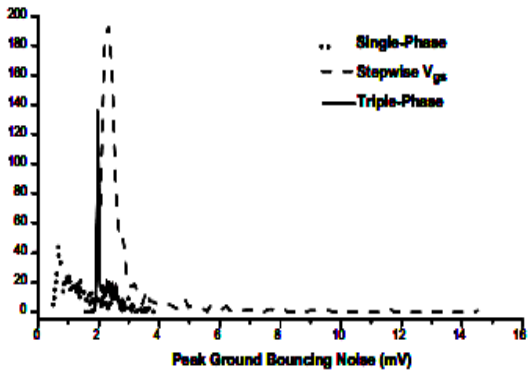

Fig.15.Statistical distribution of peak ground bouncing noise with different MTCMOS circuit techniques under within-die process variations.

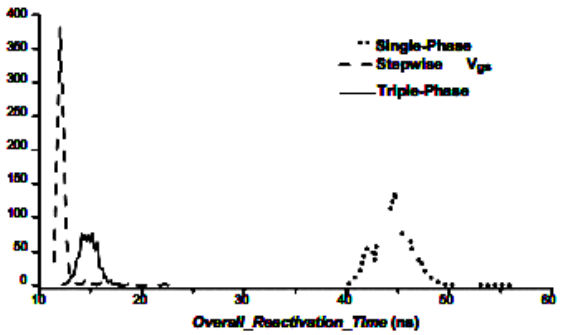

Fig.16 Statistical distribution of overall reactivation time with different MTCMOS circuit techniques under within-die process variations

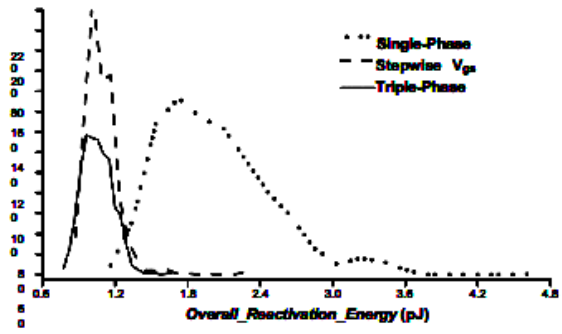

Fig.17.Statistical distribution of overallwith different MTCMOS circuit techniques under within-die process variations

In order to evaluate the overall performance of sleep signal slew rate modulated MTCMOS circuits under die-to-die and within-die process parameter variations, a comprehensive *process imperfections aware robustness metric* (*PIARM*) is evaluated next. *PIARM* is

$$PIARM = \frac{1}{N_{DEV} \times T_{R\_DEV} \times E_{R\_DEV} \times N_{SD} \times T_{R\_SD} \times E_{R\_SD}} \quad (10)$$

The normalized *PIARM* (with respect to single-phase MTCMOS circuit) is listed in Table IV. The TPS MTCMOS circuit enhances the *PIARM* by 183.1× and 54.06× as compared to the single-phase and stepwise V_{gs} sleep signal slew rate modulated MTCMOS circuits, respectively. Digital TPS is identified as the most robust technique for achieving fast and energy efficient mode transitions with negligible reactivation noise in MTCMOS circuits under process parameter fluctuations.

VI. Conclusion

Sleep signal slew rate modulation techniques are explored in this paper for reducing mode transition noise in MTCMOS circuits. A triple-phase sleep signal slew rate modulation technique with a novel digital sleep signal generator is proposed. The new digital TPS technique enhances the overall electrical quality by 9.15×4.35× and 1.21×as compared to previously published mixed-signal triple-phase, single-phase, and step wise Vgs sleep signal slew rate modulated MTCMOS circuits, respectively, under an equal-noise constraint at the typical process corner in a UMC 80-nm CMOS technology. Furthermore, the digital TPS technique is identified as the most robust MTCMOS circuit technique among the MTCMOS circuits that are evaluated in this paper under both die-to die and within-die process parameter variations. The triple phase sleep signal slew rate modulation technique enhances the overall tolerance to process parameter fluctuations by up to 183.1×and 54.06×as compared to the single-phase and stepwise Vgs sleep signal slew rate modulation techniques, respectively, based on a comprehensive robustness metric.

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