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# DIMINISHING IMPACTS OF VARIOUS OPTIMIZATION TECHNIQUES IN STRONG INVERSION AND SUBTHRESHOLD REGION AT 22NM TECHNOLOGY NODE WITH CMOS BULK MODEL

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## ABSTRACT

**The objective of the research work is to show that at advanced technology nodes like 22nm CMOS technology, the various optimization techniques have little or no impact on propagation delay, power or PDP. This is more so in the subthreshold region of 22nm technology node.HSPICE simulator has been used to simulate the NAND CMOS circuits, with and without FG technique and analyze them. Floating gate technique on CMOS NAND gate shows the reduction in power along with reduction in PDP in strong inversion region. Operation of the same circuit in subthreshold region shows the decreased power, increased delay but reduced PDP comparatively. The impact of floating gate technique is less comparatively, in subthreshold region at 22nm technology node. As expected, forward body biasing results in reduced delay and high power but the impact is less at an advanced technology node of 22nm as compared to 350nm/180nm technology. There is only 1.3% reduction in power of NAND CMOS circuit in subthreshold region with forward body bias. In subthreshold region with forward body bias, the floating gate technique has almost no impact on power and propagation delay. This experimental finding opens the future scope of the research to analyze the reasons behind the reducing impacts of optimization techniques at advanced technology nodes of 22nm or so.**

**KEYWORDS :** Floating gate technique, subthreshold region, 22nm technology, body bias, HSPICE

Floating gate CMOS circuits are for low power. These circuits can be made with standard CMOS process in which floating gate capacitance is put on the gate terminal. The net threshold voltage on the gate terminal is altered due to floating gate capacitance. The alterations of threshold voltage are due to charges on the terminal of floating gate. However these charges may leak with time through surrounding structure or very thin insulators of very advanced technology nodes [Hasler and Lande, 2001]. The purpose of the work is to show the impact of floating gate technique along with body biasing technique on 22nm circuit in super threshold region and subthreshold region. The results show that the impacts are greater in lower technology nodes compared to advanced technology nodes due to various complications arising out of advanced technology. For example body bias techniques have diminishing impact due to short channel effects. The RC combination at the gate terminal represents the leakage path of DC voltage. The charges at the capacitor also leaks due to very thin gate oxides (Naess and Berg , 2004 and Naess et. al., 2002).

Section II tells a brief on the subthreshold technique along with body bias and power, delay, PDP of various basic circuits in strong inversion and subthreshold region. It also throws light on Floating Gate circuit technique. Section III is the implementation of the 22nm NAND CMOS circuit for simulations showing the impact of Floating Gate technique and body biasing technique in super threshold and subthreshold regions using CMOS bulk model. The result shows that the impacts of the techniques are reduced as compared to older technology nodes such as 120nm or 180nm. Section IV is the conclusion.

## VARIOUS OPTIMIZATION TECHNIQUES

### Subthreshold Region And Body Bias Technique

Optimization techniques are being used in the medium range of power consumption parameter of design area and in the medium range of performance parameter (Horowitz et. al., 1994 and Chandrakasan et. al., 1992). The efforts are to study subthreshold region for ultra low power applications where performance is not very important. In subthreshold region, the subthreshold leakage current is utilized and is used as the driving current. Subthreshold current is dependent on gate voltage exponentially. This exponential dependency results in exponential reduction in the power. At the same time there is exponential increase in propagation delay. This kind of result is desirable in body wearable electronic devices such as pace maker and hearing aid (Pentland et. al., 1997 and Geddes, 1990). A subthreshold current consumes less power than strong inversion systems and circuits at the same frequency of operation.

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There has been a vast study of leakage current so that the sources of leakage currents could be identified. Also the studies have been done so that these leakage currents could be kept minimum. Then the focus shifted from minimizing the leakage current to using these leaky current to drive the logic (Kim et. al., 2003 ).

Dynamic threshold logic circuit in the subthreshold region is also an alternative logic to have logic in ultra low voltage regions. In this the substrate is tied to gate voltage. As the gate voltage changes, the substrate voltage also changes dynamically. In the ON state, body source voltage (termed as $V_{bs}$) is forward biased. This reduces the threshold of 'dynamic threshold MOS transistor (Assaderaghi et. al., 1997).

In (Soeleman and Roy,1996) the research is carried out at 0.35 μ on ultra low power digital subthreshold logic circuits. Table 1 and table2 below are the results on power, delay and PDP in strong inversion region and subthreshold region.

In (Melek et. al., 2004) subthreshold CMOS static gates are studied for body bias compensation techniques. The drain currents are dependent on process parameters that result in different NMOS and PMOS transistor drive currents. They have given new body bias compensation technique for subthreshold CMOS static logic gates. In this research work, they have provided these bias circuits that produce body biases to compensate for variations of parameters (Bryant et. al., 2001) of PMOS and NMOS transistors in static logic circuits.

**Floating Gate Mosfet Technique**

In floating gate MOSFET technology, the gate of metal oxide semiconductor transistor is isolated electrically. This gate is enveloped by resistive material and input signals are connected to gate terminal by capacitance. From DC operating point of view, the gate is floating node (Sharma et. al., 2002).

In the last 15 years floating gate circuits have improved towards a stable system with many industrial usages (Shibata and Ohmi, 1992). The research paper (Hasler and Lande,2001) shows the circuit symbol, cross section and layout for floating gate PFET device.

In floating gate technology, silicon dioxide is around a floating gate. Charges stored on the floating gate gives a permanent memory like characteristics. High class insulator surrounds the gate. The floating gate of polysilicon is not connected to any other layer but may be capacitively connected to other layers. A floating point or node is, when there is no DC path to a potential but only capacitive relation.

The charges on the floating gate decide the floating gate voltage. The floating gate voltage controls the channel between source and drain (Minch et. al., 2001).

The floating gate voltage can be written as [Inoue et. al., 2002]

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{ds} + C_{fs} V_{ss} + C_{fb} V_{bs} + Qfg}{C_T} \quad (1)$$

And $C_T$ is given as

$$C_T = \sum_{i=1}^{N} C_i + C_{fd} + C_{fs} + C_{fb} \quad (2)$$

$C_T$=Total capacitance

$C_1$, C2…..$C_N$ are the input capacitances between floating gate and control gate. is the summation of N capacitances at input.

$C_{fs}$ → overlap capacitance between source and gate (floating gate).

$C_{fb}$ → parasitic capacitances between substrate and gate (floating gate)

$V_i$ → $i^{th}$ input voltage which is at the $i^{th}$ input gate

$V_{ds}$ → drain to source voltage

$V_{ss}$ → source voltage and Vbs substrate to source voltage

$C_t$ → Total floating gate capacitance

$Q_{fg}$ → remaining charges and may be neglected during fabrication process (Villegas and Barnes, 2003)

So the equation (1) is now

$$V_{FG} = \frac{\sum_{i=1}^{N} C_i V_i + C_{fd} V_{ds} + C_{fs} V_{ss} + C_{fb} V_{bs}}{C_T} \quad (3)$$

Equations (2) (3) are reduced to

$$CT = \sum_{i=1}^{n} Ci \quad \text{and} \quad VFG = \frac{\sum_{i=1}^{N} C_i V_i}{C_T}$$

If $\sum_{i=1}^{n} Ci >> Cfd, Cfs, Cfb$

The conventional n channel MOSFET equations can be modified to get the drain current equations for NMOS with

FG technology

$$I_{ds,linear} = K_n \{[(\frac{\sum_{i=1}^{N} C_i V_i}{C_T}) - V_{ss} - V_T] V_{ds} - \frac{1}{2} V_{ds}^2\} \quad (4)$$

$$I_{ds,saturation} - \frac{Kn}{2}\{(\frac{\sum_{i=1}^{N} C_i V_i}{C_T}) - V_{SS} - V_T\}^2 \quad (5)$$

$K_n = \mu_n C_{ox} W/L$ transconductance parameter

$\mu_n$ electron mobility; $C_{ox}$ gate oxide capacitance per unit area

$W/L \rightarrow$ is width and length of a transistor

$V_T \rightarrow$ is threshold voltage of FGMOS.

In floating gate technique, the gate is in floating state. The multiple input gate is capacitively connected to floating gate. Over the N channel of MOSFET, the first layer of polysilicon makes a floating gate. The multiple input gate is formed by the 2nd polysilicon layer (Shouli and Sinencio, 2000 and Angulo et. al.,1995).

FGMOS based circuits can function at a very low supply voltage comparatively and uses very less power without compromising on the performance. FGMOS may have many inputs against 'only one' input in conventional MOS transistor (Vlassis and Siskos, 2001 and Carvajal et. al.,2003).

The formula to calculate effective gate voltage of a transistor from $V_{in}$ is [Berg and Lande, 1999]

$$Veff = Vin.\frac{Cfg}{Cfg+Cg} \quad (6)$$

## MATERIALS AND METHODS

In this research NAND CMOS (Figure 1(a) and 1(b) of figure1) is implemented and simulated with various techniques at 22nm technology node using 22nm CMOS bulk model. This CMOS NAND gate is simulated using HSPICE simulator of Synopsis and is compared with floating gate model of the same circuit. Along with this subthreshold region is also tested upon along with body biasing technique and all the results are being compared.

## RESULTS

The table 3 below shows the comparison of various optimization techniques at 22nm technology node with CMOS PTM bulk cmos model.

## DISCUSSION

The row2 of table 3 above shows that FGMOS NAND circuit the power is reduced to $1.35x10^{-8}$W compared to $2.33X10^{-8}$W. The same circuit is simulated in subthreshold region with Vdd=0.35V to show that the power is reduced many folds to $2.555X10^{-10}$W with a compromise on delay at $2.35X10^{-10}$Sec against $4.76X10^{-11}$ Sec. The impact of floating gate technique is little in subthreshold region at 22nm technology node with CMOS bulk model. The exact reason of reduced impact of floating gate technique is the future scope of this experimental work.

The experimental results show that floating gate technique at 22nm technology node shows the PDP reduction of 60.811% with respect to NAND CMOS circuit with no technique applied. The reduction in propagation delay is 25.9% in subthreshold region on applying forward body bias technique. The reduction of PDP with floating gate technique in subthreshold region is just 0.89%. The application of floating gate technique in subthreshold region results in no change in propagation delay and only 1.3% reduction in power. This is to be noted that floating gate technique at 22nm, in subthreshold region with forward body bias has almost no impact on either propagation delay or power.

**Table1: Strong inversion 35µ Hp tech Vt NMOS =0.57V, Vt PMOS=0.74V Vdd=3.3v**

| Logic | Power (Watts) | Delay (Sec) | PDP (J) |
|---|---|---|---|
| INV | 3.10x10-4 | 5.24x10-11 | 1.681x10-14 |
| NOR-2 | 4.27x10-4 | 1.24x10-11 | 5.17x10-14 |
| NAND2 | 2.24x10-4 | 9.307x10-11 | 2.087x10-14 |

**Table 2: Subthreshold region vdd=0.5v**

| Logic | Power (Watts) | Delay (Sec) | PDP (J) |
|---|---|---|---|
| INV | 5.32x10-10 | 4.493x10 | 2.392x10-16 |
| NOR-2 | 6.842x10-10 | 9.527x10 | 6.519x10-18 |
| NAND2 | 3.943x10-10 | 7.417x10 | 2.924x10-16 |

As can be seen, the optimization techniques such as floating gate or forward body biasing has the little impact at 22nm technology and further this little impact too diminishes in subthreshold region. This diminishing impact at 22nm technology in subthreshold region can be analysed further to look for the reasons. Body bias impact is reduced at advanced technology nodes due to short channel effects [Verma and Kumar, 2000 and Kumar and Verma, 2002]. There could be similar reason of reduced impact of Floating Gate technique at advanced technology nodes. One of the reasons could be leakage of the capacitor charges through thin insulators.

## CONCLUSION

In this experimental work, it is shown that floating gate technique shows an impact of reducing power in strong inversion region at 22nm technology node with CMOS bulk PTM model. But this impact is less compared to older technology nodes such as 180nm and 350nm. This impact further goes down in subthreshold region at 22nm technology which can be analysed further for the reasons, as a future scope of this research work. In subthreshold region with forward body bias, the floating gate techniques have almost no impact on power reduction at this technology node.

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**TABLE 3: comparisons of various techniques at 22nm with CMOS ptm bulk model**

| S.No. | Technique applied | Propagation Delay Sec | Power-Watts | PDP-Joules |
|---|---|---|---|---|
| 1 | Vdd-0.8V; No FG; No body bias | $4.76x10^{-11}$ | $2.33X10^{-8}$ | $11.1x10^{-19}$ |
| 2 | Vdd-0.8v;FG | $3.22x10^{-11}$ | $1.35x10^{-8}$ | $4.35x10^{-19}$ |
| 3 | Subthreshold; Vdd=0.35v | $2.35x10^{-10}$ | $2.555x10^{-10}$ | $6.0043x10^{-20}$ |
| 4 | Subthreshold; Vdd=0.35v;FBB | $1.74x10^{-10}$ | $4.36x10^{-10}$ | $7.5864x10^{-20}$ |
| 5 | Subthreshold; Vdd=0.35v; FG | $2.35x10^{-10}$ | $2.542x10^{-10}$ | $5.9737x10^{-20}$ |
| 6 | Subthreshold; Vdd=0.35v;FBB;FG | $1.74x10^{-10}$ | $4.355x10^{-10}$ | $7.5777x10^{-20}$ |

FG→Floating Gate; FBB→ forward body bias

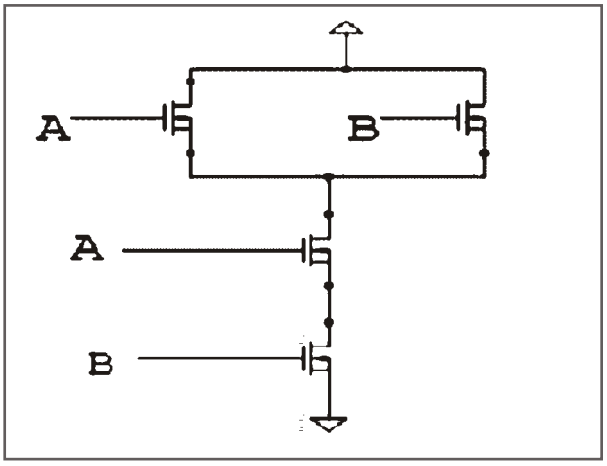


**Figure 1(a) of figure 1 NAND CMOS**

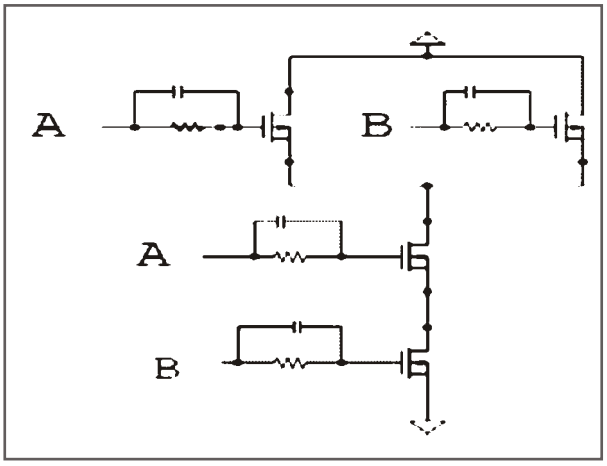


**Figure 1(b) of figure NAND FG CMOS**

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