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DESIGN AND IMPLEMENTATION OF AREA OPTIMISED GMSK COMMUNICATION SYSTEM ON FPGA

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Abstract **-** There are multitudes of modulation techniques are available for the designer of communication system. The use of particular modulation technique depends on the channel requirement This paper proposes the design and implementation of a complete communication system using the GMSK modulation scheme. The hardware is described in VHDL and implemented on SPARTAN 3E FPGA. Each block used to perform the implementation is completely described accomplishing all the requirements of this kind of modulation. Gaussian minimum shift keying modulation is a digital modulation highly used in radio communication systems due to the advantages is the spectrum efficiency provided by the Gaussian filter. The transmitter & receiver modules are described on VHDL & implemented on Spartan 3E FPGA. This paper proposes new architecture for modulators using the concept digital frequency synthesizer which maintain the low system complexity, reduce power consumption and chip area requirement.

I. Introduction

In electronics and telecommunications modulation is the process of varying one or more properties of periodic waveform called carrier signal with modulating signal which typically contains information to be transmitted. Device that performs modulation is know as modulators and device that performs the reverse is known as demodulators. In digital modulation an analog carrier signal is modulated by discrete signal. Most wireless transmission today are digital and with limited spectrum available, the type of modulation is more critical than it has ever been. The main goal of modulation today is to squeeze as much data into the least amount of spectrum possible. The spectral efficiency improved by Gaussian filter. The purpose of communication system is to transmit information bearing signal through a communication channel separating the transmitter from the & receiver. The information bearing signals are base band signal representing the original signal delivered by the source. The devolved modules of transmitter and recover are described on VHDL & implemented on FPGA [2]. There are only a few known implementations of this kind of system on FPGA [3],[4],[5],[6].The modulators are realized using the concept of direct digital frequency synthesis. The modulators concept are designed by using DDFS on the basis of hardware requirements The main design goal is to maintain low system complexity and reduce power consumption and chip area requirement[15]. Instead of a ROM LUT a hardware optimized phase to sine amplitude converter approximates the first quadrant of sine function with equal piece wise linear segments. A direct digital synthesizer in numerically controlled oscillator synthesizes a discrete-time, discrete valued representation of a sinusoidal wave form. It is an established method of generated periodic sinusoid signals whenever high frequency resolution, fast changes in frequency and phase and high spectral purity of the output signal required. In this transmitter and received blocks I used CIC filter which are multirate filter that are used for realizing large sample rate conversions in digital system This filter does not use any multipliers and consists of only adders and subtracters and registers.

II. Proposed Design

Figure 1 shows the transmitter & receiver block diagram which consists of the following blocks .such as fir filter, fm modulators & demodulators, CIC filter. On the transmitter the binary input data are presented with a 1 khz sample rate. The base band signal is filtered and converted to a higher sampling rate before being modulated onto a direct digital synthesized(DDS) carrier frequency. A direct digital synthesizer is Numerically Controlled Oscillator Synthesises a discrete-time, discrete valued representation of a sinusoidal wave form. It is an established method of generated periodic sinusoidal signals whenever high frequency resolution, fast change in frequency and phase, and spectral purity of the output signal is required. A major advantage of the DDS is that the ability to tune with extremely fine frequency and phase resolution, and to rapidly hop between frequencies. A direct digital synthesizer operates by storing the points of a wave form in the digital format and recalling them to generate the waveform. The rate at which the synthesizer completes one

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waveform then determine the frequency. The implementation of DDS can be divide in to two distinct parts namely the phase accumulator and the phase to amplitude converter

III. Transmitter Block Diagram

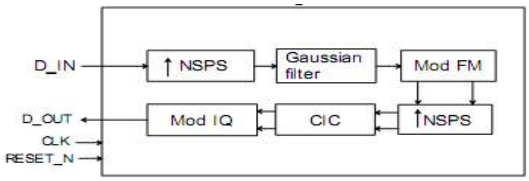

Figure 1:Transmitter Block Diagram

FIR Filter

On the transmitter, the binary input data are presented with a 1 khz sample rate. The filter represents each input symbol with 8 new samples in order to limit the bandwidth of the signal. FIR filter are implemented in Xilinx FPGA using multiply accumulator(MAC) implementation. The MAC based architecture uses a multiplier to perform the filter addition operation.MAC uses much less memory than Distributed architecture (DA) which has a heavy use of look up table.

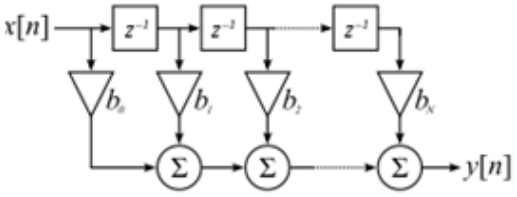

Figure 2 Structure of FIR filter

Fig2 shows a discrete-time FIR filter,where the output is a weighted sum of the current and a finite number of previous values of the input. The operation is described by the following equation, which defines the output sequence *y[n]* in terms of its input sequence *x[n]*:

$$y[n] = b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N] = \sum_{i=0}^{N} b_i x[n-i]$$

FM Modulator

This modulators modulates the incoming digital output of the filtered data Here we are using digital modulators making use of low complexity direct digital synthesizer for generating digital sine wave. Here BPSK modulation process is implemented. The frequency of the sinusoidal carrier signal is changed according to the message level(‘‘0’’ or ‘‘1’’) while keeping the amplitude and phase constant

A BPSK signal can be expressed as

$$S_{BPSK}(1) = A \sin [2\pi f_c t + m(t)\pi]$$

Where m(t)=0 or m(t)=1 the binary message ,T is the bit duration and fc,φo are the amplitude, frequency and phase of the sinusoidal carrier signal.

Implementation Of Digital Frequency Synthesizer

We use a digital frequency synthesizer in our system to generate a sampled sinusoidal wave of frequency 71 KHz estimated carrier frequency fset. The major advantage of digital frequency synthesizer is output frequency, phase and amplitude of can be precisely and rapidly manipulated under the control of DSP.

Concept Of Architecture Used

Instead of a ROM LUT, a hardware-optimized phase to sine amplitude approximates the first quadrant of the sine function with eight equal-length piecewise linear segments The main goal is to maintain low system complexity and reduce power consumption and chip area requirements The second aim is to achieve a specified spectral purity which is an essential design parameter for synthesizer used in the communication system, ensuring that undesired in-band signals remain below a given threshold In order to achieve the first goal ,I approximate a sinusoid as a series of eight equal-length piecewise continuous linear segments as shown in Table 1 where mi is the slope of each segment and is carefully selected to eliminate the requirement for multiplication by representing each one as a sum of at the most two powers of two. Equal length segments are selected to reduce the control system circuitry cost In order to achieve a desired spectral purity, different sets of mi and yi coefficients are evaluated as shown in the table offset. The major advantage of digital frequency synthesizer is output frequency, phase and amplitude can be precisely and rapidly manipulated under the control of DSP.

Table 1: Linear segment coefficients for 60 dB purity

i	m_i	y_i
0	$1+{}^1/_2$	2/1024
1	$1+{}^1/_2$	191/1024
2	$1+{}^1/_2$	384/1024
3	$1+{}^1/_8$	552/1024
4	1	697/1024
5	${}^1/_2+{}^1/_4$	819/1024
6	½	909/1024
7	${}^1/_8$	971/1024

The converter block of figure 3 includes a 1’s complement to exploit quarter wave symmetry. This architecture is less complex. It does not include a ROM no multiplexers or squaring circuits are required Equal phase to sine

amplitude length segments are used to simplify the control .Only three integers need to be added and multiplexers show in the figure have been optimized by combining similar inputs and in combinational logic The phase accumulator is 20 bit wide, truncated to 12 bits. The two msb's are used for quadrant symmetry. The remaining seven bits identify different sub-angles. The two upper multiplexers shift these remaining seven bits according to the slopes m_i listed in the table The notation {››n} indicates a right shift by n bits The lower multiplexer selects the appropriate yi listed in the table. The output from the multiplexers is 13bit wide to account for the whole dynamic range of possible values. The three operand adder sums the multiplexer outputs together and rounds the result to 15 bit.

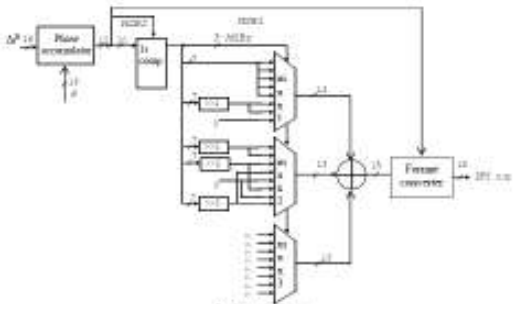

Figure 3 : DFS architecture

Cascaded Integrator-Comb Filter

A cascaded integrator-comb (CIC) is an optimized class of finite impulse response (FIR) filter combined with an interpolator or decimator.] A CIC filter consists of one or more integrator and comb filter pairs. In the case of a decimating CIC, the input signal is fed through one or more cascaded integrators, then a down-sampler, followed by one or more comb sections (equal in number to the number of integrators). An interpolating CIC is simply the reverse of this architecture, with the down-sampler replaced with a zero-stuffer (up-sampler)In transmission end upsampling is the process of inserting zero- valued samples between original samples to increase the sampling rate which is zero stuffing.

CIC filters are used in multi-rate processing. An FIR filter is used in a wide array of applications, and can be used in multi-rate processing in conjunction with an interpolator or decimator. CIC filters have low pass frequency characteristics,. CIC filters use only addition and subtraction.CIC filters are in general much more economical than general FIR filter but tradeoffs are involved. CIC has a significant advantage over a FIR filter with respect to architectural and computational efficiency

IV. Receiver Block Diagram

In the receiver block diagram consists of CIC filter consists of integrator and comb filter pair In this case decimating CIC ,the input signal is fed through integrator then a down sampler followed by comb

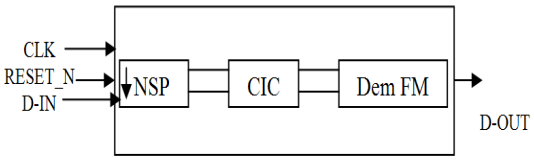

Figure 4 : Receiver block diagram

FM Demodulator

The FM demodulation recovers the base band signal. Demodulators are implemented with VHDL. Here we present a new architectures for demodulators to maintain low system complexity and reduce power consumption and chip area requirements

V. Simulation Results

The modulates-demodulators GMSK system tested using Spartan 3e FPGA. In the case of the transmitter, the number of slices used 200, available 3584 and utilization 5%, slices of used 190 available 7168 and utilization 2%, no. of 4 input LUTs used 282, available 7168 utilization 3%, No. of bounded IO's used 28 available 141 utilization 19%.

In case of receiver no of slices used 31, available 3584, utilization 0%, no of slices of flip flops used 47 available 7168 utilization 0%. No. of 4 input LUTs used 25 available 7168 utilization 0%.

FIR Filter

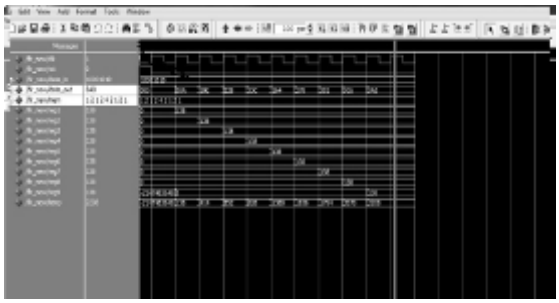

Figure 5 : Simulated output of FIR filter

Figure 6 : RTL schematic of fir filter

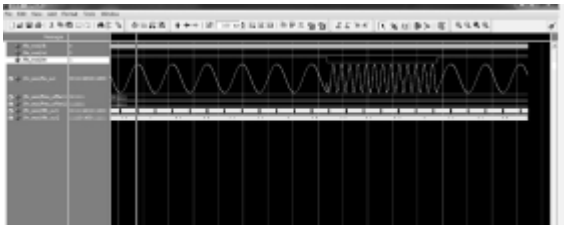

Figure 7 : Simulated output of fm modulator

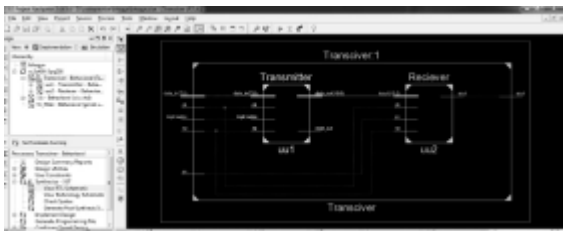

Figure 8 : RTL schematic of transceiver

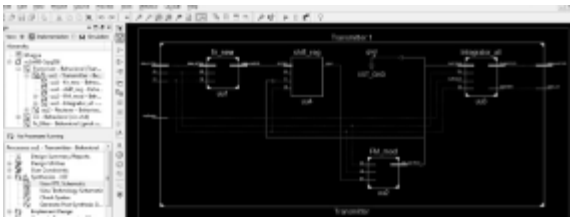

Figure 9: RTL schematic of transmitter

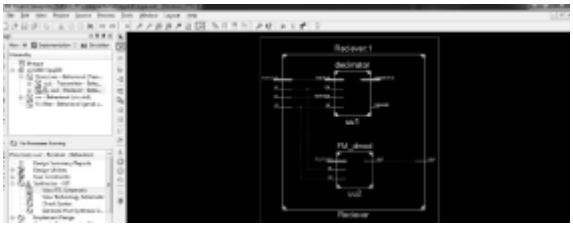

Figure 10: RTL schematic of receiver

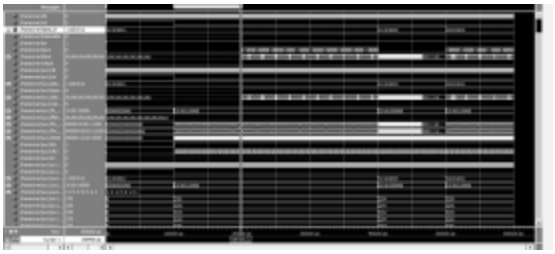

Figure 11: Final simulation of transceiver

Transciver Project Status (05/26/2013 - 09:46:25)			
Project File:	bhagya.xise	**Parser Errors:**	No Errors
Module Name:	Reciever	**Implementation State:**	Synthesized
Target Device:	xc3s400-5pq208	**• Errors:**	No Errors
Product Version:	ISE 12.2	**• Warnings:**	88 Warnings (85 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	31	3584	0%
Number of Slice Flip Flops	47	7168	0%
Number of 4 input LUTs	25	7168	0%
Number of bonded IOBs	20	141	14%
Number of GCLKs	1	8	12%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun May 26 09:46:22 2013	0	88 Warnings (85 new)	5 Infos (5 new)

Figure 12: Design summary of FIR filter

Transciver Project Status (05/26/2013 - 09:49:23)			
Project File:	bhagya.xise	**Parser Errors:**	No Errors
Module Name:	Transciver	**Implementation State:**	Synthesized
Target Device:	xc3s400-5pq208	**• Errors:**	No Errors
Product Version:	ISE 12.2	**• Warnings:**	122 Warnings (72 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	229	3584	6%
Number of Slice Flip Flops	235	7168	3%
Number of 4 input LUTs	306	7168	4%
Number of bonded IOBs	13	141	9%
Number of GCLKs	1	8	12%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun May 26 09:49:22 2013	0	122 Warnings (72 new)	5 Infos (0 new)

Figure 13: Design summary of FM modulator

Transciver Project Status (05/26/2013 - 09:38:31)			
Project File:	bhagya.xise	**Parser Errors:**	No Errors
Module Name:	Transmitter	**Implementation State:**	Synthesized
Target Device:	xc3s400-5pq208	**• Errors:**	X 1 Error (1 new)
Product Version:	ISE 12.2	**• Warnings:**	33 Warnings (31 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	200	3584	5%
Number of Slice Flip Flops	190	7168	2%
Number of 4 input LUTs	282	7168	3%
Number of bonded IOBs	28	141	19%
Number of GCLKs	1	8	12%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sun May 26 09:38:28 2013	X 1 Error (1 new)	33 Warnings (31 new)	0

Figure 14: Design summary of transmitter

FM_mod Project Status			
Project File:	fm_mod_demod.xise	**Parser Errors:**	No Errors
Module Name:	FM_mod	**Implementation State:**	Translated
Target Device:	xc3s400-5pq208	**• Errors:**	
Product Version:	ISE 12.2	**• Warnings:**	
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	113	3584	3%
Number of Slice Flip Flops	85	7168	1%
Number of 4 input LUTs	209	7168	2%
Number of bonded IOBs	18	141	12%
Number of GCLKs	1	8	12%

Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Jun 11 09:45:28 2013	0	4 Warnings (0 new)	0

Figure 15: Design summary of transceiver

VI. Conclusion

The CIC filters and Digital frequency architecture allows low complexity computation due to their multifiler less structure

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