Indian J.Sci.Res. 17(2): 65-73, 2018

ISSN: 0976-2876 (Print)
ISSN: 2250-0138(Online)

PERFORMANCE ANALYSIS OF MULTIPLEXER USING LOW POWER TECHNIQUES

[1]M Suresh, [2]Mukesh K Sukla, [3]A K Panda,
[1, 2, 3] Department. of Electronics and Communication Engineering, National Institute of Science & Technology, Berhampur

Abstract- Low power consuming devices are playing a dominant role in the present day VLSI design technology. If the power consumption is less, then the amount of power dissipation is also less. The power dissipation of a device can be reduced by using different low power techniques. In the present paper the performance of 4x1 multiplexer in different low power techniques was analyzed and its power dissipation in those techniques is compared with the conventional CMOS design. Each of these techniques has different advantages depending on their logic of operation. The simulation results show that the proposed techniques have less power dissipation compared to the conventional CMOS with reduction in area also. Gate Diffusion Input logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design.

Keywords-Power dissipation; Delay time; Reversible logic; Transistor count; PTL; DPTL; GDI; Pseudo nmos**.**

I. Introduction

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles.

Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systems constructed using irreversible hardware was demonstrated by R. Landauer in the year 1960. According to Landauer's principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmann's constant and T is the absolute temperature in Kelvin. The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods.

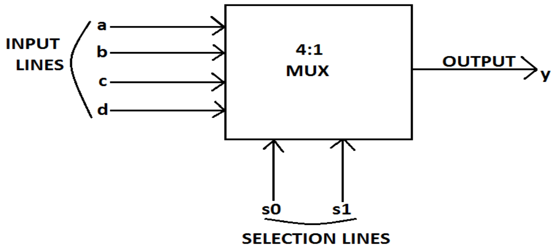
This report analyzes 4-to-1 multiplexer using different logic styles and a comparision between them using tanner tool v12.6 technology.

II. 4-to 1 Multiplexer

A multiplexer or MUX is a combinational circuit which receives binary inputs from one of the 2N input lines and it directs these inputs to a single output. The selection of a particular input data line to the output is decided by a set of selection inputs. The multiplexer or MUX is also called a data selector, because it selects one of the many input data lines and steers the binary information to the output of multiplexer.

A 4-to-1 or 4X1 multiplexer has four inputs from 'a' to 'd', two selection inputs S1 and S0and one output line Y. As we can see there are two selection inputs therefore, they can have only four possible combinations starting from 00, 01, 10 and 11. When selection inputs are 00 the input line 'a' is selected and it is directed to output. Similarly other inputs are directed one by one to the output Y for their combination of selection inputs. Its block diagram, truth table and circuit diagram is given below. The output equation of the 4X1 multiplexer is given below.

$$Y = a\overline{S0}\,\overline{S1} + b\overline{S0}S1 + cS0\overline{S1} + dSOS1$$



The expression and truth table of a 4 to 1 multiplexer is as given below.

$$Y = a\overline{S0}\,\overline{S1} + b\overline{S0}S1 + cS0\overline{S1} + dS0S1$$

SELECTION LINES		INPUTS				OUTPUT
S0	S1	a	b	c	d	Y

[1]Corresponding Author

0	0	1	0	0	0	a
0	1	0	1	0	0	b
1	0	0	0	1	0	c
1	1	0	0	0	1	d

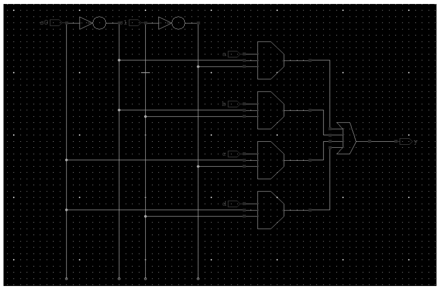
III. Design Of Mux Using Different Logic Styles

A logic style is the way how a logic function is implemented using a set of transistors. Various characteristics like speed, size, power dissipation and wiring complexity depend on a logic style and may vary considerably from one logic style to ..0another and thus choice of proper logic style is very important for circuit performance. This paper shows various logic styles to design a 4 to1 mux.

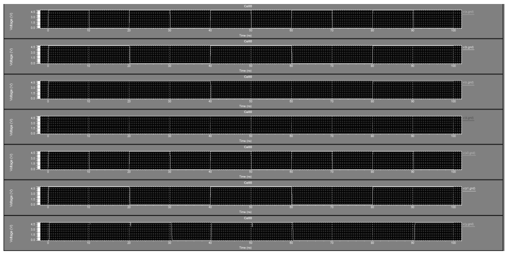
Mux using basic gates

NOT, OR and AND are the three basic gates used in designing a 4:1 multiplexer. This design uses two NOT gates, four AND gates and one OR gate. It has four inputs I0, I1, I2, I3 as data and two inputs S1 and S0 as selection lines along with a single output Y.

Implementation Of Mux Using Basic Gates:



Simulation output of mux using basic gates:



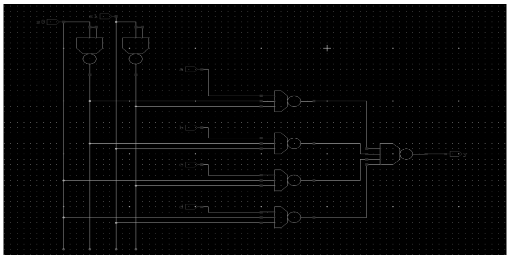
B. Multiplexer using universal gates

Multiplexers can be designed using the universal gates, i.e. the NANA only and NOR only gates.

NAND gates only

The number of transistors used in this logic is 40.

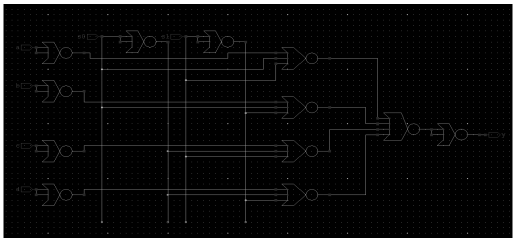
Implemantation using NAND only gates:



NOR gates only

The number of transistors used in this logic is 60.

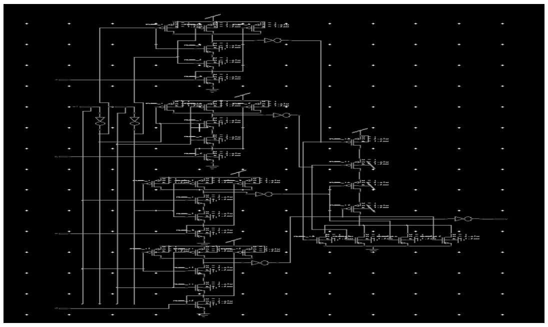
Implementation using NOR only gates:



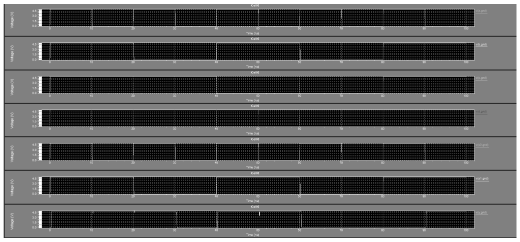
C. Mux using convensional CMOS logic

The conventional CMOS technique refers to the basic designing of Complementary Metal Oxide Semiconductor where the transistors are designed according to the basic gates. There is no separate pMOS and nMOS block for the complete circuit but they are designed at gate level:

Impementation using convensional CMOS logic:

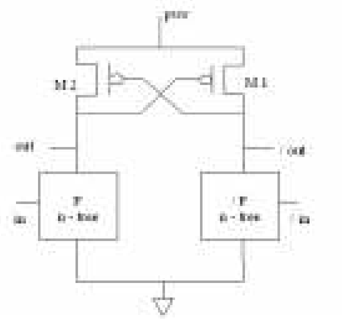


Simulation result of Impementation of mux using convensional CMOS logic:



D. Multiplexer using ECRL

ECRL stands for Efficient Charge Recovery Logic. ECRL technology is that in which precharge and evaluation simultaneously performed and by implementation of this method, energy dissipation is reduced to a large extent. ECRL eliminates the precharge diodes which causes less energy dissipation than the other adiabatic methods. It can also eliminates the need of more number of PMOS switches, only two PMOS switches are used in ECRL and it is the matter of fact that PMOS is the big source of power loss. It gives the charge on the output with full swing and it charges the load capacitance with the constant supply which is independent of the input signal.



The circuit has two cross coupled PMOS transistors M1 and M2 and two NMOS functional blocks for ECRL adiabatic logic implementation. An AC power supply power is used, so as to recover and reuse the supplied energy. Both /out and out drive a constant load capacitance independent of the input signal. The cross coupled PMOS transistors help to obtain full swing in both precharge and recover phases. ECRL always provides the charge on the output with full swing. So, the voltage on the supply clock reaches to │Vtp│and the PMOS transistor gets turned off.

Let us consider that one input is at high level and other input is at low level. At the initial cycle, when the power rises from zero to Vdd, the output remains at the ground level because it turns on the NMOS logic block. /out follows the power pwr through M1. When pwr reaches at a level of Vdd, the output holds a valid logic level. These values are restored during the hold state, and they are used as the inputs for the evaluation phase for the next stage. After the hold stage, power falls down to the ground level, /out returns its energy to the pwr so that the charge is recovered back. So, the clock powr not only acts as a clock, but also as the power supply

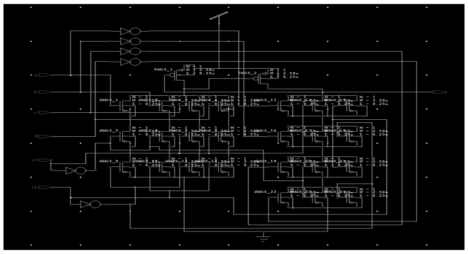
The 4*1 Multiplexer having four inputs (a,b,c and d) along with select lines(S1 and S0), we get the output Y, where,

$$Y = a\overline{S0}\,\overline{S1} + b\overline{SO}S1 + cSO\overline{S1} + dSOS1$$

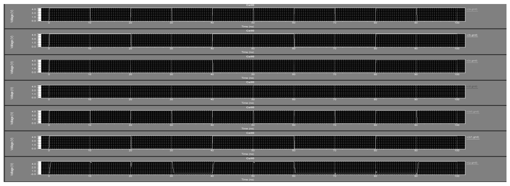
$$\overline{Y} = \overline{a\overline{S0}\,\overline{S1} + b\overline{SO}S1 + cSO\overline{S1} + dSOS1}$$

$$\overline{Y} = (\overline{a} + S0 + S1)(\overline{b} + S0 + \overline{S1})(\overline{c} + \overline{S0} + S1)(\overline{d} + \overline{S0} + \overline{S1})$$

Implementation of mux using ECRL:



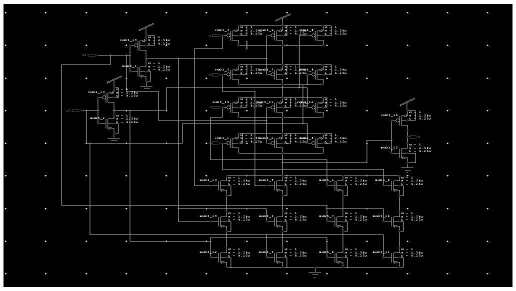
Simulation result of mux using ECRL:



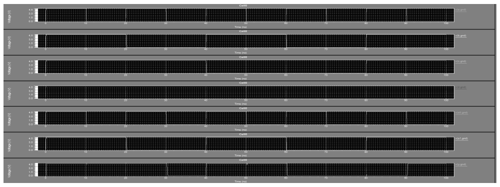
E. Multiplexer using CMOS technique

Complementary MOS is one of the most popular logic styles available today. In this logic style, both P-type and N-type transistors are used to realize logic functions. The equal signal which turns on PMOS transistor of is used to turn off NMOS transistor and vice versa. This allows the design of logic devices to be performed by using only simple switches, without a pull-up resistor . In CMOS logic gates a number of n-type MOSFETs is arranged in a pull down network between the output and the lower voltage power supply rail and the collection of p-type MOSFETs in a pull- up network between the output and higher voltage rail. Thus, when both n-type and p-type transistor have their gates connected to the same input, the one type MOSFET will be on when the another type MOSFET is off. The CMOS technology refers to the Complementary Metal Semiconductor logic, which is different from the conventional CMOS technique on basic of design of transistors. The overall pMOS circuit is designed simultaneously at the top in this case and similarly the overall nMOS circuit is designed at the bottom and the output comes from the junction of the pMOS and nMOS block.

Implementation of mux using CMOS logic:



Simulation result of mux using CMOS logic:



F. Multiplexer using Reversible logic

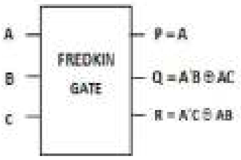
A reversible logic gate is an n-input and n-output logic device which have one-to-one mapping internally. This helps to determine the outputs from the inputs and the inputs can also be recovered from the outputs uniquely. Also in the synthesis of reversible circuits direct fan-Out is not allowed as it is one to many concept, wich is not reversible. However fan-out in reversible circuits is achieved using additional gates.The combination of output signal at any instance can provide the exact status of input combination.

In the proposed 4:1 multiplexer we have used Fredkin gates.

Fredkin Gate :

The Fredkin gate is a 3*3 gate. The input vector is IN(A, B, C) and the output vector is OUT (P, Q, R). The output is defined by P=A, Q=A′B   AC and R=A′C   AB. Quantum cost of a Fredkin gate is 5.

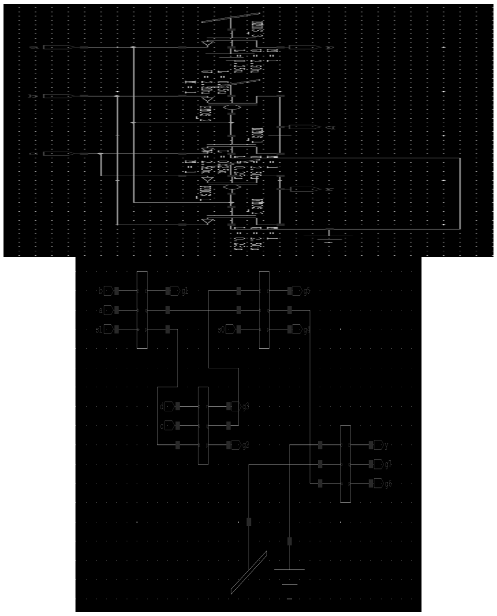
Block diagram of a Fredkin gate



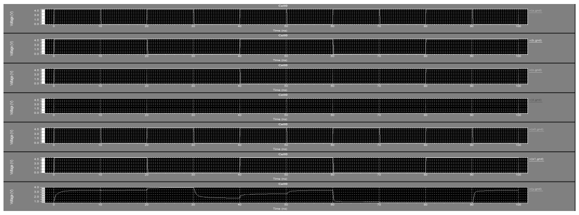
Truth table of Fredkin gate

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	**1**	**1**	**1**	**1**	**1**

Implementation of mux using reversible gate

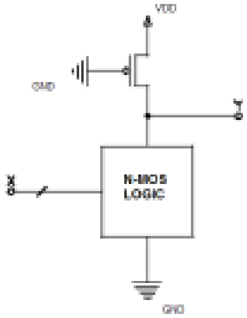


Simulation results of mux using reversible gates:



G. Multiplexer usingPseudo nMOS logic

Pseudo nMOS technology refers to use of a PMOS transistor simply as a pull-up device for an n-block. The block diagram is given as:

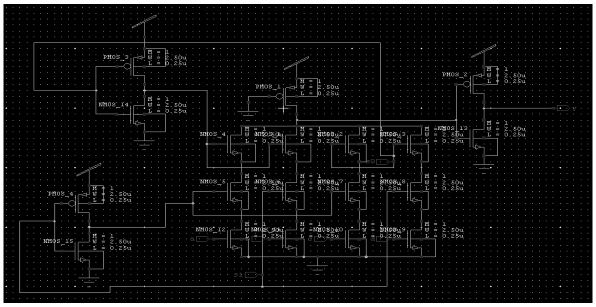


This type of logic is not ratio-less, i.e., the transistor's width must be chosen properly, i.e., The pull-up transistor must be chosen wide enough to conduct a multiplication of the n-block's leakage and narrow enough so that the n-block can still pull down the output safely.

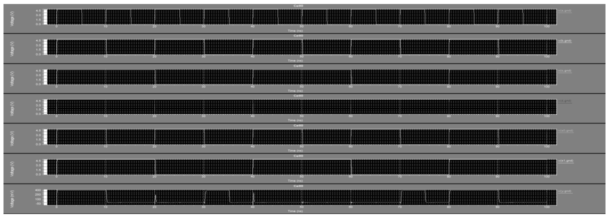
$$I_{off,n}F_{in} < W_pI_{on,p} < I_{on,n}/F_{in}$$

The pseudo-NMOS logic are advantageous in the field of its speed (these are high speed especially, in large-fan-in NOR gates) and low transistor count. The negative side is static power consumption of the pMOS transistor acting as pull-up transistor and the reduced gain and output voltage swing, which makes the gate more susceptible to noise. Again, when pseudo-NMOS logic is combined with static CMOS in only time critical signal paths, the overall improvement of speed can be substantiated at the cost of only a slight increase of static-power consumption. Furthermore, when the pull-up transistor gate is connected to an appropriate control signal it can be turned off, i.e., pseudo-NMOS supports a power-down mode at no extra cost.

Implementation of mux using Pseudo nMOS logic:



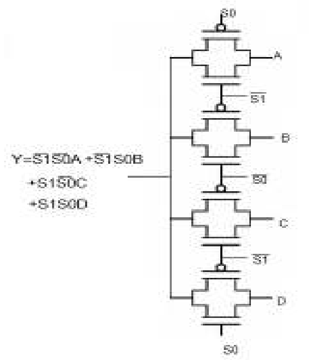
Simulation result of mux using Pseudo nMOS logic:



H. Multiplexer using transmission gates (TG)

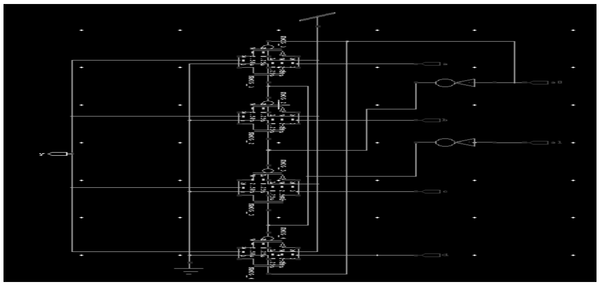
A Transmission Gate or TG is a CMOS switch. It is an electronic element and good non mechanical relay which are built with CMOS technology. The transmission gate is made by parallel combination of nMOS and pMOS transistors with the input at the gate of one transistor is complementary to the input at the other gate's input.

The transmission gate has two states i.e. both transistors acts simultaneously i.e. one is both are ON and one OFF simultaneously. The NMOS switch will pass good zero but a poor 1. The PMOS switch passes a good one and a poor 0.

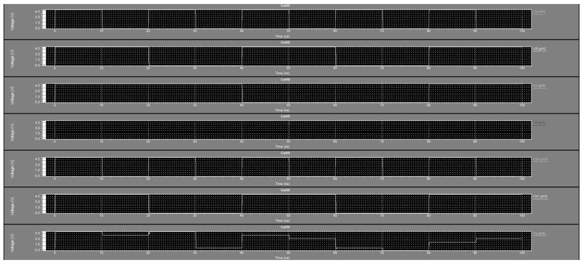


The use of transmission gates in circuit deigns decreases the total transistor count causing diminish in power dissipation and also enhances the delay.

Implementation of mux using transmission gates:



Simulation results of mux using transmission gates:



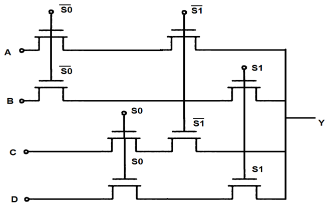
I. Multiplexer using pass transistor logic (PTL)

PTL or Pass transistor logic describes several logic families which are used in the designing of integrated circuits. It reduces the count of transistors to make various logic gates, by eliminating some redundant transistors. Transistors are used as switches to pass transistor logic levels between nodes of a circuit, instead of switches connected directly to supply voltages. It reduces the number of active devices to be used, but has the the difference of the voltage between high and low logic levels decreases at each stage which is a disadvantage. Each transistor in series is less saturated at its output port than at its input port. If several devices are chained in series in a logic path, a gate, which is conventionally constructed may be required to restore the voltage of signal to the full value. By contrast, CMOS logic switches transistors so that the output will connect to one of the power supply rails, so logic voltage levels in a sequential chain will not decrease. Circuit simulation may be required to ensure adequate performance.

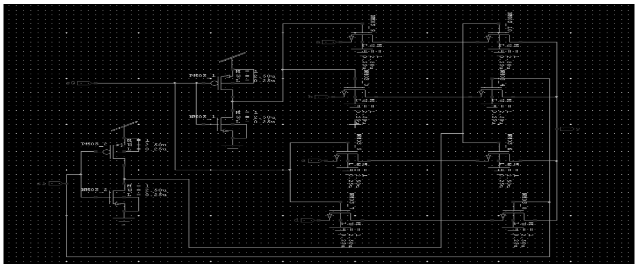
The pass-transistor logic reduces the transistor count required to implement logic by allowing the primary inputs to drive gate, source and drain. A single pass-transistor network (either NMOS or PMOS) is sufficient to perform a logic operation. Some pass logic styles such as NMOS Pass Transistor Logic, CMOS Transmission logic, and pass transistor logic are considered for implementation of 2-to 1 multiplexer. Among all of these logics NMOS Multiplexer is optimized. It uses only 2 NMOS transistors and these two pass-transistors at the input select which signal to propagate.

The circuit function in Pass Transistor Logic is implemented as a tree consisting of pull-down and pull-up branches. Since the NMOS transistor threshold voltage drop degrades the "high" level of pass-transistor output nodes, the output signals are restored by CMOS inverters. This logic use s only nMOS transistors and the circuit operations is followed by the value of inputs given at gate source and drain terminals of nMOS.

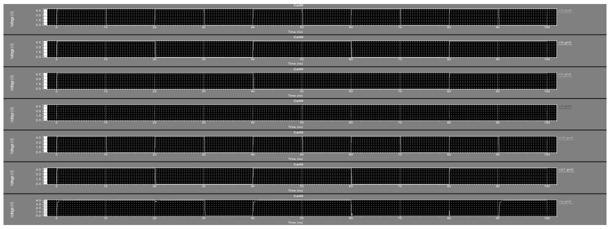
The 4:1 multiplexer can be designed using 8 nMOS transistors and the data and selection line inputs are as given in the figure below:



Implementation of mux using Pass Transistor Logic:



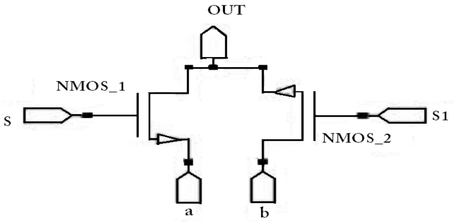
Simulation result of mux using pass transistor logic:



J. Multiplexer *using modified nMOS logic:*

The word nMOS logic refers to the method of using only nMOS transistors in forming a circuit. In conventional nMOS technology, the whole nMOS based circuit is designed according to the rules of CMOS logic and a nMOS was connected on the top of the circuit with the gate of that nMOS giving output. Its advantages were transistor count minimization and less power consumption. As the circuit replaced the huge number of pMOS transistors the transistor count decreased. Since pMOS causes greater power dissipation as compared nMOS it is beneficial to use nMOS logic.

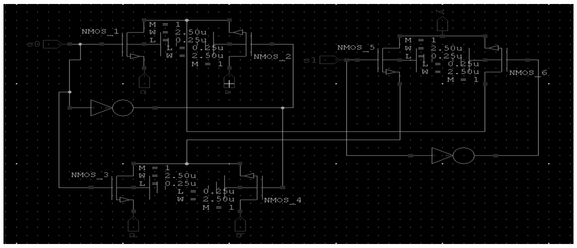
The logic diagram of Modified NMOS 2:1 MUX is shown in Figure below:



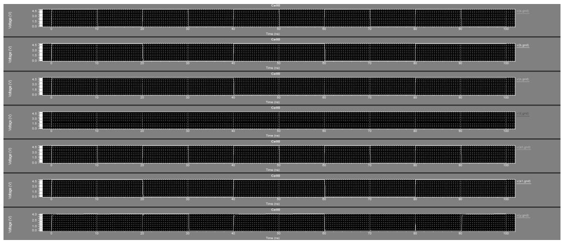
There are two select lines S, S1 and inputs are a, b, where S1 is the complementary signal of S Gate terminals of NMOS are connected to select lines. The circuit is based on Complementary Pass Transistor Logic.

Thus, in the modified nMOS logic, the design uses very less number of transistors with respect to conventional nMOS technology. In the proposed design, three 2:1 multiplexers used in order to form a 4:1 multiplexer.

Implementation of mux using modified nmos technique:



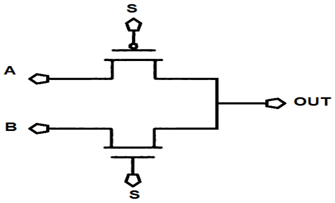
Simulation result of mux using modified nmos:



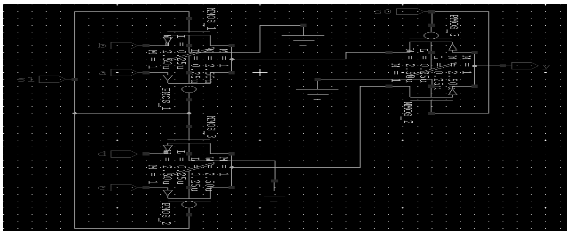
K. Multiplexer using DPTL logic

The Dual Pass Transistor Logic (DPTL) is a powerful configuration in CMOS technologies. DPTL buffers have the ability to generate standard CMOS levels regardless of input signal variation. A basic DPTL structure consists of pMOS and nMOS transistors connected in parallel to each other. The exchange of NMOS and PMOS, VDD and GND generates Dual logic function in DPTL.

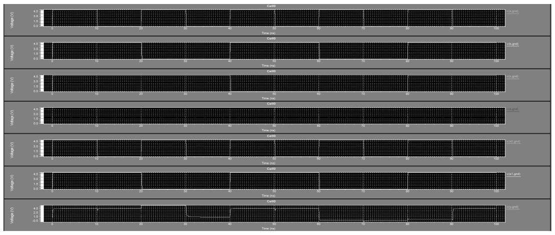
The basic structure of a DPTL cell is given beow:



Implementation of mux using DPTL:



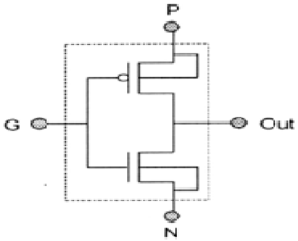
Simulation result of mux using DPTL*:*



L. Multiplexer using GDI Logic

GDI or Gate Diffusion Input logic circuits provide some major issues of enhanced hazard tolerance and operation at low voltage of reversible logic circuits. The new proposed design technique will consume less power than the other traditional gate. In GDI cell PMOS is not connected to supply voltage and NMOS is not grounded, rather they are connected as inputs.

The basic cell is similar to one of the standard CMOS inverter, but there are some important differences. A basic GDI cell contains 3 inputs, given as: G (common gate input of nMOS and pMOS), N (input to the source/drain of nMOS) and P (input to the source/drain of pMOS). The basic GDI cell is as given below:



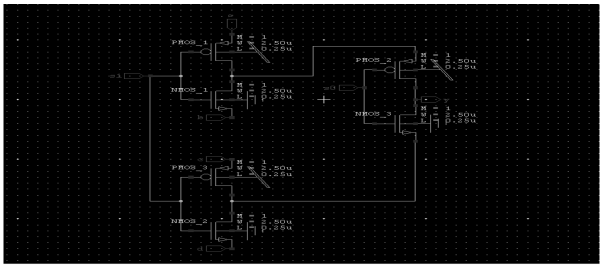
It must be remarked that all of the functions are not possible in standard p-well CMOS but can be successfully implemented in silicon on insulator (SOI) technologies. One of the major problems of Gate-diffusion input technique requires a special CMOS process. GDI schemes require twin-well CMOS process to implement the design. It is more expensive than other standard cell. The GDI is effective in low power, low leakage current and power delay.

The function table, showing behavior of the basic GDI cell is given below:

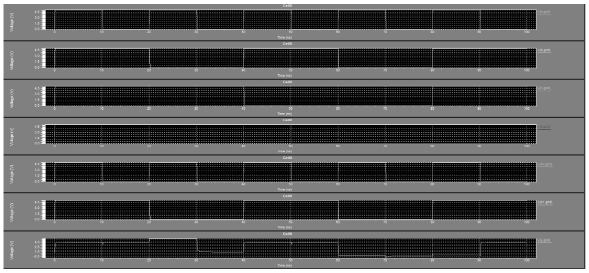
INPUTS			OUTPUT	
N	P	G	OUT	Function
0	B	A	ĀB	F1
B	1	A	Ā+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	ĀB+AC	MUX
0	1	A	Ā	NOT

The proposed 4:1 multiplexer is formed two GDI 2:1 multiplexers. We have used three 2:1 multiplexers made in GDI technique to implement the 4 to 1 multiplexer.

Implementation of mux using GDI logic*:*



Simulation result of mux using GDI*:*



IV. Results And Discussion

This section deals with the tabular representation of the logic styles with the different parameters in terms of the transistor count, power dissipation & delay. This 4:1 multiplexer was simulated using tanner tool v12.6 technology to get the values.

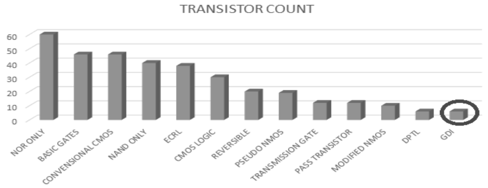
A. Tabular representation of parametric variation

The table below shows the transistor count, delay & power for different logics styles.

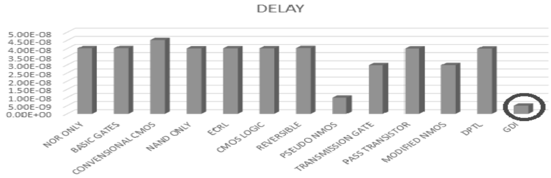
B. Graphical representation of parametric variation

This section deals with the graphical comparison of the logic styles with the different parameters in terms of the transistor count, delay & power dissipation.

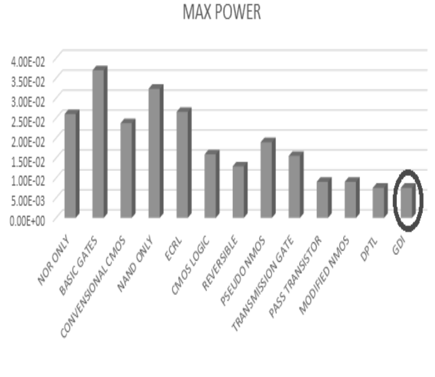
Graph for Logic style Vs Total count of transistors:

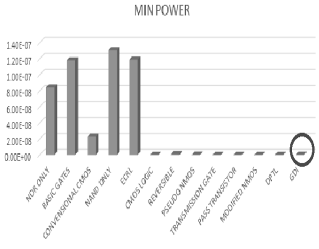


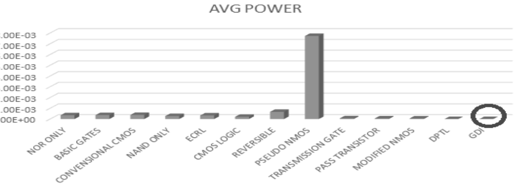
Graph for Logic style Vs Total delay:



Graph for Logic style Vs Maximum, Minimum and Average powers:







V. Conclusion

From the work carried out in this project for implementation of 4 to 1 Multiplexer, we conclude that use of Gate Diffusion Input (GDI) logic style for implementation of 4 to 1 multiplexer provides improvement in power consumption, delay and transistor count when compared with implementation with other logic styles. From the simulation and results using S-edit of tanner tool it is observed the GDI and DPTL techniques are efficient for low power consumption, while GDI is more efficient in the field of delay. These techniques will let the circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Though the design of hardware costs incurred in near future may be high but the power cost and performance is more dominant than logic hardware cost in today's computing era, so the need of low power techniques cannot be ignored.

References

[1] Vandana Shukla, O. P. Singh, G. R. Mishra, R. K. Tiwari, "Multiplexer Circuit Using Reversible Logic" *International Journal of Computational Engineering Research*, Vol, 03.Issue, 10 Novel Design of A 4:1.

[2] Prashant R. Yelekar & Prof. Sujata S. Chiwande, "Introduction to Reversible Logic Gates & its Application" *2nd National Conference on Information and Communication Technology (NCICT)*, 2011 *Proceedings published in International Journal of Computer Applications® (IJCA)*.

[3] Y.Syamala and A.V.N.Tilak, "Synthesis of Multiplexer and Demultiplexer Circuits using Reversible Logic," *Int. J. of Recent Trends in Engineering and Technology*, Vol. 4, No. 3, Nov 2010 © 2010 ACEEE DOI: 01.IJRTET.04.03.12034 .

[4] M. Burmester and Y. Desmed, "Efficient Design of Reversible Multiplexers with Low Quantum Cost and Power Consumption*," International Journal of Emerging Technology and Advanced Engineering,* Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Issue 7, July 2014).

[5] Ira Parashar, Preeti Sikarwar, Rashmi Singh, Soumya Chauhan, Mrs. Shivani Saxena, "Design And Simulation Of 4*1 Mux Based On Low Power Design Techniques," *SSRG International Journal of VLSI & Signal Processing (SSRG-IJVSP)* – volume 2 Issue 2 March-April 2015 ISSN: 2394 - 2584 Available: www.internationaljournalssrg.org Page 6.

[6] Satish Sharma, Shyam Babu Singh & Shyam Akashe, "A Power Efficient GDI Technique for Reversible Logic Multiplexer of Emerging Nanotechnologies" *International Journal of Computer Applications* (0975 – 8887) Volume 73– No.14, July 2013.